ANNA UNIVERSITY, CHENNAI

UNIVERSITY DEPARTMENTS

M.E. VLSI DESIGN AND EMBEDDED SYSTEMS

REGULATIONS – 2023

CHOICE BASED CREDIT SYSTEM

VISION OF DEPARTMENT OF ELECTRONICS ENGINEERING

The Department of Electronics Engineering is committed to produce globally competitive and socially sensitized graduates in Electronics & Communication Engineering. We seek to instill the spirit of creativity and leadership skills enabling the students to make a global impact towards the availability of technology to mankind from all walks of life.

MISSION OF DEPARTMENT OF ELECTRONICS ENGINEERING

- To impart high quality technical education to students from socially and economically diverse backgrounds
- Give solid foundation on Mathematical skills and allied fields of Electronics & Communication
- To produce students with technical competence to design sophisticated systems in Electronics & Communication
- To make high quality research contribution in the field of Electronics, Communication, Networking , VLSI & Signal Processing
- To collaborate with industries in Electronics & Communication in the indigenous product development
- To inculcate qualities of leadership and entrepreneurship in students
- To facilitate adequate exposure to the faculty enabling them to be synchronized with the Cutting edge technology

PROGRESS THROUGH KNOWLEDGE

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1. PROGRAMME EDUCATIONAL OBJECTIVES(PEOs):

I. Enrich students to excel in research leading to cutting edge technology in VLSI design and Embedded Systems and creating competent, innovative, and productive professionals in this field.

II. Provide students with a solid foundation in MOS devices, digital electronics design, analog system design and computer architecture principles leading to VLSI design

III. Understand the various applications and employ Embedded Systems based solutions to them with good scientific and engineering knowledge so as to comprehend, analyze, design, and create novel products for real life problems.

IV. Provide dynamic diverse academic environment to the students and aware of excellence, leadership, ethical conduct, positive attitude, societal responsibilities and lifelong learning needed for a successful professional career and to Inculcate entrepreneurial skills to start industries related to VLSI design and embedded system technologies.

2. PROGRAMME OUTCOMES(POs):

PO#	Programme Outcomes
1	An ability to independently carry out research/investigation and development work to solve practical problems
2	An ability to write and present a substantial technical report/document
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program.
4	Ability to design and conduct experiments, perform analysis, applying the knowledge of computing, mathematics, science and electronic engineering for designing VLSI and Embedded Systems.
5	Interpret the problems of VLSI and Embedded Systems and investigate solutions and work towards improved solutions.
6	Continuously update knowledge with modern tools and technical developments and ensure professional development.

PROGRAMME SPECIFIC OUTCOMES (PSOs):

By the completion of VLSI Design and Embedded Systems programme, students will have the following programme specific outcomes

I. Foundation of VLSI systems: Ability to understand the fundamentals of VLSI systems. Students can assess the basic components and modules of VLSI systems.

II. Foundation of Embedded Systems: Ability to understand the basic principles of Embedded Systems. Students can assess the basic components and modules of Embedded Systems.

III. Foundation of Mathematical concepts: Ability to apply mathematical knowledge to solve complex computations related to the field of VLSI and Embedded Systems.

IV. Applications of VLSI Design and Research ability: Ability to use knowledge in various domains to identify research gaps and hence provide solutions with innovation.

V. Identify the research gaps and provide innovative solutions.

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PEO/PO Mapping:

PEO	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
I.	3	1	3	3	3	3
II.	3	1	3	3	3	3
III.	3	1	3	3	3	3
IV.	2	1	3	2	2	2

PROGRAM ARTICULATION MATRIX OF M.E. VLSI DESIGN AND EMBEDDED SYSTEMS

		COURSE NAME	PO1	PO2	PO3	PO4	PO5	PO6
YEAR I	SEMESTER I	Advanced Applied Mathematics	3	1	2	3	1	1
		Research Methodology and IPR	2.2	1.8	1	3	2	1.2
		Digital Integrated Circuit Design	3	1	2	3	3	1
		VLSI Architectures for System Design	3	1	3	3	2	1
		Advanced Embedded System Design	1.6	3	2.4	2	1.6	1.4
		Embedded Internet of Things	1.6	2.2	2.4	1.8	1.6	1.4
		Advanced Digital VLSI Lab	3	2	3	3	2	2
	SEMESTER II	Design for Testability	2.6	1	1.6	1.8	1.6	1
		CMOS Analog IC Design	3	1	3	3	2	1
		Computer Vision and Embedded AI	2.4	2.4	2.4	1.8	1.8	1.4
		VLSI Signal Processing Techniques	3	1	3	3	2	1
		Embedded Automation	1.8	2.4	2.2	1.8	1.6	1.2
		Professional Elective I						
		Analog System Design Lab	3	2.4	3	3	1.8	2
YEAR II	SEMESTER III	Professional Elective II						
		Professional Elective III						
		Professional Elective IV						
		Project Work I	3	3	3	3	3	3
	SEMESTER IV	Project Phase II	3	3	3	3	3	3

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PROGRAM ELECTIVE COURSES(PEC)							
		PO1	PO2	PO3	PO4	PO5	PO6
1	ASIC Design	1.4	2.5	2.5	2.2	1	-
2	Real Time Systems	1.8	2.6	3	1.8	1.8	1
3	Real Time Operating Systems	3	1	3	2.6	2.4	1.8
4	Digital Image and Video Processing	3	1	3	1.6	1.6	2.2
5	Micro Electro Mechanical Systems and Microsystems	1	1.4	3	1.8	1.4	1
6	Adaptive Signal Processing Techniques	3	1	2	2	1	1.4
7	VLSI For Wireless Communication	3	1	3	2	2	1
8	Computer Aided Design for VLSI Systems	2.4	1	1.8	1.4	1.4	1.2
9	Hardware Software Co-Design of Embedded System	2.8	1	2.8	2.8	2.8	2
10	Embedded Networking	2.2	1	2.4	2.6	1.8	1.4
11	Quantum Computing	3	1	2.2	2	1	1
12	Multi-Core Architectures andProgramming	3	1	2.4	1	2	1
13	RF IC Design	3	1	3	2	2	1
14	Advanced CMOS Analog ICDesign	3	1	3	1.6	1.6	1
15	SoC Design for EmbeddedSystem	3	1	2.4	2	1	1
16	Robotics	3	1	3	3	3	1.8
17	Embedded C Programming	2.8	1	2.8	2.6	2	1.4
18	Digital Signal Processors andArchitectures	3	1	2.8	3	2	1
19	Reconfigurable Architectures and Applications	3	1	2.8	1.4	1.6	1
20	Pattern Recognition and Machine Learning	2	1.4	1.4	2	2.4	2.4
21	Energy Efficient VLSI Design	3	3	3	2.8	1	-
22	Solid State Device Modeling	3	1	3	3	2	1
23	Network on Chip Design	3	1	2.2	1.8	1.2	1
24	Distributed EmbeddedComputing	3	1	2.4	1.8	1	1.2
25	Embedded AutomotiveSystems	2.4	1	2.8	2.6	2.2	1.4
26	ComputationalIntelligence	3	2	3	1.6	2	2
27	Electromagnetic Interference and Electromagnetic Compatibility	2.8	1	2.8	2.8	2.8	2.8
28	Signal Integrity for High Speed Electronic Systems	3	1	1.6	1.8	1	1

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CURRICULA AND SYLLABI
SEMESTER I

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PERWEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	MA3152	Advanced Applied Mathematics	FC	4	0	0	4	4
2.	RM3151	Research Methodology and IPR	RMC	2	1	0	3	3
3.	VE3101	Digital Integrated Circuit Design	PCC	3	0	0	3	3
4.	VE3102	VLSI Architectures for System Design	PCC	3	0	0	3	3
5.	VE3103	Advanced Embedded System Design	PCC	3	0	2	5	4
6.	VE3104	Embedded Internet of Things	PCC	3	0	2	5	4
PRACTICALS								
7.	VE3111	Advanced Digital VLSI Laboratory	PCC	0	0	4	4	2
			TOTAL	**18**	**1**	**8**	**27**	**23**

SEMESTER II

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PERWEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VE3201	Design for Testability	PCC	3	0	0	3	3
2.	VE3202	CMOS Analog IC Design	PCC	3	0	0	3	3
3.	VE3203	Computer Vision and Embedded AI	PCC	3	0	2	5	4
4.	VE3204	VLSI Signal Processing Techniques	PCC	3	0	0	3	3
5.	VE3205	Embedded Automation	PCC	3	0	2	5	4
6.		Professional Elective I	PEC	3	0	0	3	3
PRACTICALS								
7.	VE3211	Analog System Design Laboratory	PCC	0	0	4	4	2
			TOTAL	**18**	**0**	**8**	**26**	**22**

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SEMESTER III

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.		Professional Elective II	PEC	3	0	0	3	3
2.		Professional Elective III	PEC	3	0	0	3	3
3.		Professional Elective IV	PEC	3	0	0	3	3
PRACTICALS								
4.	VE3311	Project Work I	EEC	0	0	12	12	6
			TOTAL	**9**	**0**	**12**	**21**	**15**

SEMESTER IV

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
PRACTICALS								
1.	VE3411	Project Work II	EEC	0	0	24	24	12
TOTAL				**0**	**0**	**24**	**24**	**12**

TOTAL NO. OF CREDITS: 72

FOUNDATION COURSES (FC)

S. NO.	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			PERIODS PER WEEK	SEMESTER
			L	T	P		
1.	MA3152	Advanced Applied Mathematics	4	0	0	4	1

PROFESSIONAL CORE COURSES (PCC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			L	T	P		
1.	VE3101	Digital Integrated Circuit Design	3	0	0	3	1
2.	VE3102	VLSI Architectures for System Design	3	0	0	3	1
3.	VE3103	Advanced Embedded System Design	3	0	2	4	1
4.	VE3104	Embedded Internet ofThings	3	0	2	4	1
5.	VE3201	Design for Testability	3	0	0	3	2
6.	VE3202	CMOS Analog IC Design	3	0	0	3	2
7.	VE3203	Computer Vision and Embedded AI	3	0	2	5	4
8.	VE3204	VLSI Signal ProcessingTechniques	3	0	0	3	2
9.	VE3205	Embedded Automation	3	0	2	4	2

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10	VE3111	Advanced Digital VLSI Laboratory	0	0	4	2	1
11	VE3211	Analog System Design Laboratory	0	0	4	2	2
					TOTAL CREDITS	**35**	

RESEARCH METHODOLOGY AND IPR COURSES (RMC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			L	T	P		
1.	RM3151	Research Methodology and IPR	2	1	0	3	1
					TOTAL CREDITS		**3**

PROGRAM ELECTIVES

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1	VL3051	ASIC Design	PEC	3	0	0	3	3
2	VE3051	Real Time Systems	PEC	3	0	0	3	3
3	VE3001	Real Time Operating Systems	PEC	3	0	0	3	3
4	NE3053	Digital Image and Video Processing	PEC	3	0	0	3	3
5	VE3002	Micro Electro Mechanical Systems and Microsystems	PEC	3	0	0	3	3
6	NE3251	Adaptive Signal Processing Techniques	PEC	3	0	0	3	3
7	VE3003	VLSI for Wireless Communication	PEC	3	0	0	3	3
8	VE3004	Computer Aided Design for VLSI Systems	PEC	3	0	0	3	3
9	VE3005	Hardware Software Co-Design of Embedded System	PEC	3	0	0	3	3
10	VE3006	Embedded Networking	PEC	3	0	0	3	3
11	VE3007	Quantum Computing	PEC	3	0	0	3	3
12	VE3008	Multi-Core Architectures and Programming	PEC	3	0	0	3	3
13	WT3055	RF IC Design	PEC	3	0	0	3	3
14	VE3009	Advanced CMOS Analog IC Design	PEC	3	0	0	3	3
15	VE3010	SoC Design for Embedded System	PEC	3	0	0	3	3
16	VE3011	Robotics	PEC	3	0	0	3	3
17	VE3012	Embedded C Programming	PEC	3	0	0	3	3
18	VE3013	Digital Signal Processors and	PEC	3	0	0	3	3

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		Architectures						
19	VE3014	Reconfigurable Architectures and Applications	PEC	3	0	0	3	3
20	WT3053	Pattern Recognition and MachineLearning	PEC	3	0	0	3	3
21	VE3015	Energy Efficient VLSI Design	PEC	3	0	0	3	3
22	VE3016	Solid State Device Modeling	PEC	3	0	0	3	3
23	VE3017	Network on Chip Design	PEC	3	0	0	3	3
24	VE3018	Distributed Embedded Computing	PEC	3	0	0	3	3
25	VE3019	Embedded Automotive Systems	PEC	3	0	0	3	3
26	NE3052	Computational Intelligence	PEC	3	0	0	3	3
27	NE3054	ElectromagneticInterference andElectromagnetic Compatibility	PEC	3	0	0	3	3
28	WT3058	Signal Integrity For High Speed Electronic Systems	PEC	3	0	0	3	3

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	VE3311	Project Work I	0	0	12	6	3
2.	VE3411	Project Work II	0	0	24	12	4
TOTAL CREDITS						18	

SUMMARY

	NAME OF THE PROGRAMME: M.E VLSI DESIGN AND EMBEDDED SYSTEMS					
	SUBJECT AREA	CREDITS PER SEMESTER				CREDITS TOTAL
		I	II	III	IV	
1.	FC	4	0	0	0	4
2.	PCC	16	19	0	0	35
3.	PEC	0	3	9	0	12
4.	RMC	3	0	0	0	3
5.	EEC	0	0	6	12	18
6.	**TOTAL CREDIT**	**23**	**22**	**15**	**12**	**72**

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MA3152 **ADVANCED APPLIED MATHEMATICS** **L T P C**
4 0 0 4

UNIT I LINEAR ALGEBRA 12

Vector spaces – norms – Inner Products – Eigenvalues using QR transformations – QR factorization - generalized eigenvectors – Canonical forms – singular value decomposition and applications - pseudo inverse – least square approximations --Toeplitz matrices and some applications.

UNIT II ONE DIMENSIONAL RANDOM VARIABLES 12

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT III RANDOM PROCESSES 12

Classification – Auto correlation - Cross correlation - Stationary random process – Markov process –- Markov chain - Poisson process – Gaussian process.

UNIT IV LINEAR PROGRAMMING 12

Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models

UNIT V FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS 12

Fourier transforms: Definitions, properties-Transform of elementary functions, Dirac Delta functions – Convolution theorem – Parseval‘s identity – Solutions to partial differential equations: Heat equations, Wave equations, Laplace and Poisson‘s equations.

TOTAL: 45+15=60 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

CO1 Apply the concepts of linear algebra to solve practical problems.
CO2 Use the ideas of probability and random variables in solving engineering problems.
CO3 Classify various random processes and solve problems involving stochastic processes.
CO4 Formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
CO5 Apply the Fourier transform methods of solving standard partial differential equations.

REFERENCES:

1. Andrews, L.C. and Philips.R.L., “Mathematical Techniques for engineering and scientists”, Printice Hall of India, New Delhi, 2006.
2. Bronson, R., “Matrix Operation”, Schaum‘s outline series, Tata McGrawHill, New York, 2011.
3. O‘Neil P.V., “Advanced Engineering Mathematics”, Cengage Learning, 8th Edition, India, 2017.
4. Oliver C. Ibe, “Fundamentals of Applied Probability and Random Processes”, Academic Press, Boston, 2014.
5. Sankara Rao, K., “Introduction to partial differential equations”, Prentice Hall of India, pvt, Ltd, 3rd Edition, New Delhi, 2010.
6. Taha H.A., “Operations Research: An introduction”, Ninth Edition, Pearson Education, Asia, 10th Edition, New Delhi, 2017.

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CO-PO Mapping:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	2	2
CO2	3	3	3	3	2	2
CO3	3	3	3	3	2	2
CO4	3	3	3	3	2	2
CO5	3	3	3	3	2	2
AVG	3	3	3	3	2	2

RM3151 RESEARCH METHODOLOGY AND IPR L T P C
2 1 0 3

UNIT I RESEARCH PROBLEM FORMULATION 9

Objectives of research, types of research, research process, approaches to research; conducting literature review- information sources, information retrieval, tools for identifying literature, Indexing and abstracting services, Citation indexes, summarizing the review, critical review, identifying research gap, conceptualizing and hypothesizing the research gap

UNIT II RESEARCH DESIGN AND DATA COLLECTION 9

Statistical design of experiments- types and principles; data types & classification; data collection - methods and tools

UNIT III DATA ANALYSIS, INTERPRETATION AND REPORTING 9

Sampling, sampling error, measures of central tendency and variation,; test of hypothesis- concepts; data presentation- types of tables and illustrations; guidelines for writing the abstract, introduction, methodology, results and discussion, conclusion sections of a manuscript; guidelines for writing thesis, research proposal; References – Styles and methods, Citation and listing system of documents; plagiarism, ethical considerations in research

UNIT IV INTELLECTUAL PROPERTY RIGHTS 9

Concept of IPR, types of IPR – Patent, Designs, Trademarks and Trade secrets, Geographical indications, Copy rights, applicability of these IPR; , IPR & biodiversity; IPR development process, role of WIPO and WTO in IPR establishments, common rules of IPR practices, types and features of IPR agreement, functions of UNESCO in IPR maintenance.

UNIT V PATENTS 9

Patents – objectives and benefits of patent, concept, features of patent, inventive steps, specifications, types of patent application; patenting process - patent filling, examination of patent, grant of patent, revocation; equitable assignments; Licenses, licensing of patents; patent agents, registration of patent agents.

TOTAL: 45 PERIODS

COURSE OUTCOMES

Upon completion of the course, the student can

CO1: Describe different types of research; identify, review and define the research problem

CO2: Select suitable design of experiment s; describe types of data and the tools for collection of data

CO3: Explain the process of data analysis; interpret and present the result in suitable form

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CO4: Explain about Intellectual property rights, types and procedures
CO5: Execute patent filing and licensing

REFERENCES:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education, 11e (2012).
2. Soumitro Banerjee, “Research methodology for natural sciences”, IISc Press, Kolkata, 2022,
3. Catherine J. Holland, “Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets”, Entrepreneur Press, 2007.
4. David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
5. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.

VE3101 DIGITAL INTEGRATED CIRCUIT DESIGN L T P C
3 0 0 3

UNIT I MOS TRANSISTOR PRINCIPLES 9

MOS Technology and VLSI, CMOS fabrication process and Electrical properties of CMOS circuits – Secondary effects – Device modeling – Process variations – Static and Dynamic behavior of CMOS inverter – Power and Energy – Scaling Principles – Stick Diagram – layout diagram

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Static CMOS logic design - Complementary CMOS – logical effort – sizing - Ratioed logic – Pass transistor Logic. Dynamic CMOS logic – principles – speed and power dissipation – signal integrity issues – cascading dynamic gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS AND MEMORY ARRAY STRUCTURES 9

Static and Dynamic Latches and Registers, Timing Issues, Pipelines, Clocking strategies, Design of Memory and array structures - Memory Architectures, Memory Core - Memory control circuits.

UNIT IV DATAPATH SUBSYSTEMS 9

Datapath circuits : Architectures for Adders - Accumulators – Multipliers -Shifters - Barrel Shifters – Logarithmic Shifters - Need for testing -Manufacturing test – Design for testability – Boundary scan Speed and Area tradeoffs.

UNIT V IMPLEMENTATION STRATEGIES 9

DIGITAL: Full custom and semicustom design – cell based design – array based implementation - Programmable ASIC logic cells - ACTEL ACT - Xilinx LCA - Altera FLEX and MAX.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Understand the basics of MOS devices, CMOS Inverters
CO2: Design different types CMOS combinational circuits and sequential circuits
CO3: Design various memory architectures
CO4: Design and analyze different datapath/arithmetic circuits and understand testing in VLSI circuits
CO5: Understand different FPGA architectures and implementation Logic circuits using FPGAs.

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REFERENCES:

1. Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated circuits: A design perspective”. Second Edition, Prentice Hall of India, 2016.
2. N.Weste, D.M.Harris, “CMOS VLSI Design: Circuits and System Perspective”, Fourth Edition, Pearson, 2015.
3. N.Weste, K.Eshraghian, “Principles of CMOS VLSI Design”, A system Perspective, second edition,Addision Wesley 2010.
4. M.J. Smith, “Application specific integrated circuits”, Addisson Wesley, 2009.
5. A.Pucknell, Kamran Eshraghian, “Basic VLSI Design”, Third edition, Prentice Hall of India, 2007.
6. R.Jacob Baker, Harry W.LI., David E.Boyee, “CMOS Circuit Design, Layout and Simulation”, Prentice Hall of India, 2005.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	2	3	1	1
CO2	3	1	2	3	3	1
CO3	3	1	2	3	3	1
CO4	3	1	2	3	3	1
CO5	3	1	2	3	3	1
AVG	15/5=3	5/5=1	10/5=2	15/5=3	12/4=3	5/5=1

VE3102 VLSI ARCHITECTURES FOR SYSTEM DESIGN L T P C
3 0 0 3

UNIT I VERILOG HDL IN SYSTEM DESIGN 9

Overview - Evolution of Computer-Aided Digital Design -Typical Design Flow -Basic Concepts - Lexical conventions, data types, system tasks, compiler directives - Gate-Level Modeling - Dataflow Modeling -behavioral Modeling -Tasks and Functions -Design Example.

UNIT II PROGRAMMABLE LOGIC DEVICES 9

Logic implementation options - Technology trends - Design with Field Programmable devices - ROM, PLA, PAL - CPLD - XC9500 family - Erasable Programmable Logic Devices - MAX5000, MAX7000 families.

UNIT III FPGA AND FPAA 9

Programming Technology, Logic blocks, routing architectures of SRAM-Programmable FPGA Architectures - XC2000, XC3000, XC4000 - Antifuse Programmed FPGAs - Routing Architecture of the Actel FPGAs – Pro ASIC plus - Design Applications - Current FPGA Technologies - FPAA architecture and its reconfiguration.

UNIT IV SYNCHRONOUS FSM DESIGN 9

Choice of Components to be Considered - Architecture Centered around Nonregistered PLDs - State Machine Designs - Centered around a Shift Register, Centered around a Parallel Loadable Up/Down Counter - One hot design method - Use of Algorithmic State Machine, Application of one hot design to serial 2's complementer, parallel to serial adder/subtractor controller- System-level design: controller, data path, and functional partition.

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UNIT V ASYNCHRONOUS STATE MACHINE DESIGN 9

Features and need for Asynchronous FSMs - Lumped path delay models for asynchronous FSMs - Excitation table, state diagrams, K-maps, and state tables - Design of the basic cells by using the LPD model - design examples - Hazards in Asynchronous FSMs - One-hot design of asynchronous state machines - Design of fundamental mode FSMs by using PLDs.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Implement the digital designs with programmable logic devices
CO2: Analyze the architectural features of FPGA and FPAA
CO3: Make the system level designs using synchronous and asynchronous FSMs
CO4: Design the fundamental mode FSMs using PLDs
CO5: Apply pulse mode approach to FSM Design

REFERENCES:

1. M. Morris Mano and Michael D. Ciletti, 'Digital Design', Pearson, 6th Edition, 2018
2. Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated circuits: A design perspective". Second Edition, Prentice Hall of India, 2016.
3. Stephen M.Trimberger, Edr.,"Field Programmable Gate Array Technology", Springer Science- Business media, LLC, 2012.
4. P.K.Chan& S. Mourad, "Digital Design Using Field Programmable Gate Array", Pearson, 2009
5. Roger Woods, John McAllister, Gaye Lightbody and Ying Yi, "FPGA-based implementation of Signal Processing Systems", A John Wiley and Sons, Ltd., Publication, 2008.
6. John V. Oldfield, Richard C.Dorf, "Field Programmable Gate Arrays - Reconfigurable logic for rapid prototyping and implementation of digital systems", John Wiley & Sons, Reprint, 2008.
7. Samir Palnitkar,"Verilog HDL: A Guide To Digital Design And Synthesis",Second Edition,Prentice Hall of India, 2003.
8. Richard F.Tinder, "Engineering Digital Design, Revised Second Edition", Academic Press, 2000.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	3	3	2	1
CO2	3	1	3	3	2	1
CO3	3	1	3	3	2	1
CO4	3	1	3	3	2	1
CO5	3	1	3	3	2	1
AVG	15/5=3	5/5=1	15/5=3	15/5=3	10/5=2	5/5=1

VE3103 ADVANCED EMBEDDED SYSTEM DESIGN L T P C
3 0 2 4

UNIT I PIC 16F877 MICROCONTROLLER AND RTOS 9+6

Features – Architecture – Memory Organization – I/O Ports – Timers – Capture/Compare/PWM –

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Interrupts – ADC – Master Synchronous Serial Port – USART – WatchDog Timer – Reset – Real time Operating Systems – Multithreaded Programming - Scheduling – Resource Sharing – Memory Management.

UNIT II ASSEMBLY LANGUAGE AND EMBEDDED C 9+6

Instruction Set – Assembly Language Programming - Embedded C Program Structure – Datatypes and Variables – C Statements, Structures and Operators – Functions and Procedures - Structures and union – Development Tools – MikroC – Language Reference - Standard Libraries – User Defined Libraries – Optimizing and Testing Embedded C Programs.

UNIT III CONFIGURING AND PROGRAMMING PERIPHERALS 9+6

LED – LCD – Seven Segment Display – Dot Matrix Displays – Keypad – Keyboard - Sensors – Motors (DC, Stepper, Servo) – Real Time Clock – Timers/Counters – CCP Module – Interrupt – MSSP Module (I2C, SPI) - USART – RTOS Programming

UNIT IV SIMPLE EMBEDDED SYSTEM DESIGN PROJECTS 9+6

Chasing LEDs – LED Dice – Bank Visitor Seven Segment LED Counter – Voltmeter with LCD – Calculator with LCD and Keypad – Serial Communication based Calculator – Speed Control of DC Motor – Robotic 4-wheel Car - Controlling High Powered Devices – Rangefinder – Multiprocessor Communication.

UNIT V ADVANCED EMBEDDED SYSTEM DESIGN PROJECTS 9+6

Water Level Notifier/Controller – Elevator Design – Data Logger with SD Card – Home Automation – Proximity Garage Door Open/Close System – Package Delivery Detector – Curtain Automation – CAN based Automation - AI and IoT enabled Embedded Systems.

TOTAL: 45 + 30 = 75 PERIODS

LIST OF EXPERIMENTS

1. Interfacing basic digital input output devices
2. Interfacing a character LCD
3. Interfacing A/D and D/A converter
4. Interfacing Capture/Compare/PWM module
5. DC motor control
6. Multiplexing seven segment LED displays
7. Interfacing Stepper motor and temperature sensor
8. Traffic light controller using IDE
9. Water Level Notifier/Controller
10. Elevator Design

COURSE OUTCOMES:

CO1: To be able to explain the concepts of PIC16F877 microcontroller and RTOS.
CO2: To be able to perform microcontroller programming using ASM and Embedded C.
CO3: To be able to configure and program the peripherals connected to PIC16F877 MCU.
CO4: To be able to apply the design skill in building simple embedded systems.
CO5: To be able to design advanced real time embedded systems

REFERENCES:

1. Dogan Ibrahim, “Advanced PIC Microcontroller Projects in C – From USB to RTOS with the PIC18F Series”, Newnes Publions – Elsevier, 2008.

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2. Muhammad Ali Mazidi, Rolin McKinlay, Danny Causey, "PIC Microcontroller and Embedded Systems: Using Assembly and C for PIC18", Prentice Hall publications, 2007.
3. Martin Bates, “Interfacing PIC Microcontrollers – Embedded Design by Interactive Simulation”, Newnes Publication – Elsevier, 2006.
4. “User Manual - C Compiler for Microchip PIC Microcontrollers – mikroC”, Mikroelectronika, 2006.
5. Kirk Zurell, “C Programming for Embedded Systems”, R & D Books, 2000.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	1	3	2	1	1	1
CO2	1	3	2	1	1	1
CO3	1	3	2	2	1	1
CO4	2	3	3	3	2	1
CO5	3	3	3	3	3	3
AVG	8/5=1.6	15/5=3	12/5=2.4	10/5=2	8/5=1.6	7/5=1.4

VE3104 EMBEDDED INTERNET OF THINGS L T P C
3 0 2 4

UNIT I INTRODUCTION 9+6

IoT Definition and Characteristics - Levels of IoT Deployment - IoT Device Management - M2M Communication - IoT Enabling Technologies - Standardized Architecture - Core IoT Functional Stack - Cloud in IoT, Functional blocks of an IoT ecosystem. IoT based Monitoring Device Development (multiparameter)

UNIT II PROTOCOLS – DATALINK LAYER AND NETWORK LAYER 9+6

Physical and MAC Layer: 3GPP MTC - IEEE 802.11 - IEEE 802.15 - Wireless HART - ZWave - Bluetooth Low Energy - Zigbee - LORA WAN.

Network Layer: IPv4 - IPv6 - 6LoWPAN, 6TiSCH - DHCP - ICMP - CORPL- CARP wireless LAN Technology.

UNIT III PROTOCOLS – TRANSPORT, SESSION AND APPLICATION LAYER 9+6

Transport Layer: TCP – MPTCP – UDP – DCCP – SCTP – TLS - DTLS – SCADA.

Session Layer: HTTP - CoAP - XMPP – AMQP - MQTT Service Layer Protocol & Security - Service Layer one M2M - ETSI M2M - OMA-BBF Security in IoT Protocols MAC 802.15.4 - 6LoWPAN – RPL.

Application Layer: - CoAP and MQTT

UNIT IV EMBEDDED IOT SYSTEM HARDWARE AND TOOLS 9+6

IoT Supported Development Boards – Arduino - Node MCU ESP8266 – Raspberry Pi – Odroid XU4 – Jetson Nano - Porting OS – Peripheral Interfacing (Input Devices, Output Devices, Sensors, Actuators) – Communication Protocols - Open-Source Packages and Development Environments – Cloud Connectivity – IoT Gateway - Enabling RTOS – Scheduling. Machine to Machine Communication

UNIT V CASE STUDIES 9+6

Smart Home Automation – Smart Healthcare - Smart Cites – Smart Agriculture – Smart

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Transportation-Smart Parking System

LIST OF EXPERIMENTS

1. IoT based Monitoring Device Development (multiparameter)
2. Smart Home
3. Smart Energy meter
4. Smart City
5. Smart Transportation
6. Smart Agriculture
7. Smart Healthcare
8. Smart Environment
9. Smart Parking system
10. Machine to Machine Communication

COURSE OUTCOMES:

CO1: To be able to explain the fundamental concepts in Internet of Things.
CO2: To be able to detail about the different protocols supported in Datalink and Network layer.
CO3: To be able to elucidate the different protocols related to Transport, Session and Application layer.
CO4: To be able to develop an Embedded IoT device.
CO5: To be able to design and develop Embedded IoT systems for challenging applications.

REFERENCES:

1. Pethuru Raj and Anupama C. Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press,2017
2. Constandinos X. Mavromoustakis, George Mastorakis, Jordi Mongay Batalla, “Internet of Things (IoT) in 5G Mobile Technologies” Springer International Publishing Switzerland 2016.
3. Vijay Madisetti and Arshdeep Bahga, “Internet of Things (A Hands-on Approach)”, VPT, 1st Edition, 2014.
4. Honbo Zhou, “Internet of Things in the cloud:A middleware perspective”, CRC press, 2012.
5. Dieter Uckelmann, Mark Harrison, Florian Michahelles, “Architecting the Internet of Things” Springer-Verlag Berlin Heidelberg, 2011.

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CO1	1	2	2	1	1	1
CO2	1	2	2	1	1	1
CO3	1	2	2	1	1	1
CO4	2	2	3	3	2	2
CO5	3	3	3	3	3	2
AVG	8/5=1.6	11/5=2.2	12/5=2.4	9/5=1.8	8/5=1.6	7/5=1.4

VE3111 ADVANCED DIGITAL VLSI LABORATORY L T P C
0 0 4 2

PART 1 MODULE DESIGN USING FPGA IMPLEMENTATION (VERILOG/VHDL):

1. Design of 8-bit serial and parallel adder and 8-bit multipliers.
2. Design of 8:1 Multiplexer using universal gates and realization of Full Adder using Multiplexers.

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3. Design of 4-bit code converter and 4-bit Magnitude compactor.
4. Design of Design of 8-bit Fixed point Arithmetic logical Unit.
5. Design of Universal shift registers
6. Design of Synchronous and Asynchronous Counters.
7. Design of Finite State Machine (Moore/Mealy)
8. Design of Memories.

PART 2 APPLICATIONS BASED MODULE DESIGN USING FPGA IMPLEMENTATION

1. Design of Smart watch system using HDL.
2. Design of Traffic light controller using HDL.
3. Design of washing machine controller using HDL.
4. Design of Elevator design using HDL.
5. Design of Vending machine design using HDL.
6. Design of Micro oven controller using HDL

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Write HDL code for basic as well as advanced digital integrated circuit
CO2: Import the logic modules into FPGA Boards
CO3: Synthesize Place and Route the digital ICs
CO4: Design various digital IC blocks
CO5: Design, Simulate and Extract the layouts of Digital ICs

TOTAL: 60 PERIODS

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	2	3	3	2	2
CO2	3	2	3	3	2	2
CO3	3	2	3	3	2	2
CO4	3	2	3	3	2	2
CO5	3	2	3	3	2	2
AVG	15/5=3	10/5=2	15/5=3	15/5=3	10/5=2	10/5=2

VE3201 DESIGN FOR TESTABILITY L T P C
3 0 0 3

UNIT I INTRODUCTION TO TESTING 9

Importance of testing - Testing during the VLSI life cycle - Challenges and levels of abstraction in VLSI testing - VLSI Technology Trends Affecting Testing -Types of testing. Fault Models - Defects, errors, Faults -Stuck-At Faults - Fault Equivalence, Fault Collapsing, Fault Dominance- Transistor Faults, Open and Short Faults, Delay Faults, Pattern Sensitivity and Coupling Faults - Analog Fault Models- Automatic test Equipment.

UNIT II LOGIC AND FAULT SIMULATION 9

SCOAP Testability Analysis **-** Algorithms for True Value simulation **-** Compiled-Code Simulation, Event-Driven Simulation - Algorithms for Fault Simulation - Serial Fault Simulation, Parallel Fault Simulation, Deductive Fault Simulation,- Concurrent fault simulation Roths TEST-DETECT Algorithm.

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UNIT III ATPG FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Combinational Circuit: Algorithms and Representations, Redundancy Identification (RID), Combinational ATPG Algorithms - D-Calculus and D-Algorithm, PODEM and FAN.

Sequential Circuit: ATPG for Single-Clock Synchronous Circuits, Time-Frame Expansion Method, Simulation-Based Sequential Circuit ATPG -CONTEST Algorithm, Genetic Algorithm.

UNIT IV DFT METHODS AND BUILT-IN SELF-TEST 9

DFT Methods - Ad Hoc Approach, Structured Approach - Scan Cell Designs - Scan Architectures - Scan Design Rules - Scan Design Flow.

BIST - Design Rules - Test Pattern Generation - Output Response Analysis - Logic BIST Architectures - Fault Coverage Enhancement - BIST Timing Control - Logic BIST System Design - A Design Practice - Memory BIST.

UNIT V BOUNDARY SCAN STANDARD AND CORE-BASED TESTING 9

Core-Based Design and Test Considerations - Digital Boundary Scan - IEEE Std. 1149.1 - Test Architecture and Operations, Test Access Port and Bus Protocols, Data Registers and Boundary-Scan Cells, TAP Controller - Embedded Core Test Standard (IEEE Std. 1500) - Architecture, Wrapper Components and Functions - Comparisons between 1500 and 1149.1 Standards

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design and simulate the fault models
CO2: Apply fault simulation algorithms for circuit under test
CO3: Design test pattern generation circuits for combinational and sequential circuits
CO4: Design built-in-self test for circuit under test
CO5: Analyze the testability techniques for Embedded core design

REFERENCES:

1. M.L. Bushnell, V. D. Agrawal, “Essentials of electronic testing for digital memory and mixed Signal VLSI Circuits - Kluwer Academic Publishers, Reprint 2013.
2. L.T. Wang, C.W. Wu and X. Wen, VLSI Test Principles and Architectures, Elsevier, 2006.
3. AlexanderDigitalMiczo,LogicTesting“ and Simulation”, Second Edition , A jhon Wiley &sonsInc. Publication, 2003.
4. Alfred Crouch, “Design for test for digital IC & Embedded Core Systems”,Prentice Hall, 2002.
5. Samiha Mourad, Yervant Zorian, “Principles of Testing Electronic Systems” A WileyInterscience Publications, 2002.
6. Abramovici, M, Breuer, M.A and Friendman, A.D., ”Digital systems and Testing and Testable Design”,Computer Science Press, 1994

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CO 1	1	1	1	1	1	3
CO 2	1	1	3	1	1	3
CO 3	1	2	3	3	1	3
CO 4	1	2	1	2	1	2
CO 5	1	2	1	1	1	2
AVG	5/5=1	8/5=1.6	9/5=1.8	8/5=1.6	5/5=1	13/5=2.6

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3 0 0 3

UNIT I SINGLE STAGE AMPLIFIERS 9

Review of MOS physics and equivalent circuits and models. Large and Small signal analysis CS, CG and source follower, miller effect, frequency response of CS, CG and source follower.

UNIT II CURRENT MIRRORS 9

Current Sources, Basic Current Mirrors, Current steering circuit, Cascode stages for Current mirrors, Wilson Current Mirror, Wilson Current Mirror Large and small signal analysis of current mirrors.

UNIT III MULTISTAGE DIFFERENTIAL AMPLIFIERS 9

Differential amplifier, Large and small signal analysis of the balanced differential amplifier, device mismatches in differential amplifier, small and large signal analysis of the differential pair with current mirror load, $PSRR^+$, $PSRR^-$ and CMRR of differential amplifiers, small signal analysis of telescopic amplifier, two-stage amplifier and folded cascoded amplifier.

UNIT IV FREQUENCY RESPONSE OF MULTISTAGE DIFFERENTIAL AMPLIFIERS 9

Frequency response of differential amplifier-transfer function method, Miller effect, Dominant-Pole approximation, Upper Cutoff frequency-zero-value time constant method,UGF-short circuit time constant method, frequency response of telescopic cascoded, folded cascaded and two-stage amplifiers.

UNIT V STABILITY AND FREQUENCY COMPENSATION OF FEEDBACK AMPLIFIERS9

Properties and types of negative feedback circuits, feedback configurations, effect of loading in feedback networks, feedback circuit analysis using return ratio modelling input and output port in feedback network, the relation between gain and bandwidth in feedback amplifiers, phase margin, frequency compensation, compensation of two stage MOS amplifiers.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze and design CMOS analog IC building blocks
CO2: Design the various current mirror biasing circuits
CO3: Analyze and Design the various single and multistage differential amplifier architectures
CO4: Analyze the frequency response of single and multi-stage differential amplifiers
CO5: Analyze and design various feedback amplifiers with compensation

REFERENCES:

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, 2nd Edition, Tata McGraw Hill, 2017.
2. Gray, Hurst, Lewis, Meyar, “Analysis and Design of Analog Integrated Circuits” Fifth Edition John Wiley, 2016.
3. Phillip E. Allen, Douglas R.Holberg, “CMOS Analog Circuit Design”, Third edition, Oxford University Press, 2011.
4. Jacob Baker “CMOS: Circuit Design, Layout, and Simulation, Third Edition”, Wiley IEEE Press 2010.
5. Kenneth William Martin, David Johns, “Analog Integrated Circuit Design”, Wiley India, 2008.

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	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	3	3	2	1	3
CO 2	1	3	3	2	1	3
CO 3	1	3	3	2	1	3
CO 4	1	3	3	2	1	3
CO 5	1	3	3	2	1	3
AVG	5/5=1	15/5=3	15/5=3	10/5=2	5/5=1	15/5=3

VE3203 COMPUTER VISION AND EMBEDDED AI L T P C
3 0 2 4

UNIT I COMPUTER VISION 9+6

Image – Formation – Processing –Structuring Element – Morphological Operations - Kernel – Blurring and Sharpening – Thresholding – Gradients – Canny Edge Detector – Image Descriptors – Feature Descriptors – Color Histogram – Haralick Texture – Local Binary Pattern – HoG - Feature Detection and Matching.

UNIT II MACHINE LEARNING 9+6

Definition – Types – Steps in Machine Learning Process – Performance Metrics - k Nearest Neighbor – k means Clustering – Support Vector Machine – Logistic Regression – Decision Tree – Random Forest – Naïve Bayes – Multilinear Regression – Principal Component Analysis – Tools and Libraries

UNIT - III DEEP LEARNING 9+6

Neural Network - Multilayer Perceptron – Backpropagation Algorithm - Convolutional Neural Network – Parameter Estimation and Optimization – Transfer Learning – Pretrained Models - Recurrent Neural Network – LSTM – GRU – Reinforcement Learning – Tools and Libraries.

UNIT – IV EMBEDDED SYSTEM DEVELOPMENT 9+6

Open Source Packages and Development Environments - GPU/TPU Supported Boards – Porting OS – Peripheral Interfacing (Input Devices, Output Devices, Sensors, Actuators) – Camera Interface - Porting Machine Learning/Deep Learning Algorithms – Enabling RTOS – Scheduling – GPU Parallel Computing – Computing Strategy.

PROGRESS THROUGH KNOWLEDGE

UNIT – V CASE STUDIES 9+6

Hand Written Digit Classification using Neural Network and CNN - Regression – Face Detection in Images and Videos – Object Detection and Tracking in Video – Gesture Recognition – Automatic License Plate Recognition – Semantic Segmentation - Text Classification – Image Captioning Unauthorized Entry Identifier-Automatic Guided Vehicle-IoT based multi-Parameter Monitoring System-Smart Attendance System-Smart Surveillance System

TOTAL: 45 +30 = 75 PERIODS

LIST OF EXPERIMENTS:

1. Hand Written Digit Classification using Neural Network
2. Hand Written Digit Classification using CNN
3. Regression
4. Face Detection in Images and Videos
5. Object Detection and Tracking in Video

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6. Gesture Recognition
7. Automatic License Plate Recognition
8. Semantic Segmentation
9. Text Classification
10. Image Captioning
11. Unauthorized Entry Identifier
12. Automatic Guided Vehicle
13. IoT based multi-Parameter Monitoring System
14. Smart Attendance System
15. Smart Surveillance System

COURSE OUTCOMES:

CO1: To be able to explain the fundamental concepts in Computer Vision.
CO2: To be able to detail about the different machine learning algorithms.
CO3: To be able to elucidate the concept of Neural Network and related architectures.
CO4: To be able to develop a Machine Learning/Deep Learning based standalone Embedded AI system.
CO5: To be able to apply the Embedded AI skill in developing real time applications.

REFERENCES:

1. Avimanyu Bandyopadhyay, "Hands-on GPU Computing with Python", Packt Publishing, 2019.
2. Salman Khan, Hossein Rahmani, Syed Afaq Ali Shah and Mohammed Bennamoun, "A Guide to Convolutional Neural Networks for Computer Vision", Morgan & Claypool Publishers, 2018.
3. Adrian Rosebrock, "Deep Learning for Computer Vision with Python", PyImageSearch, 2017.
4. Kevin P. Murphy, "Machine Learning – A Probabilistic Perspective", The MIT Press Cambridge, Massachusetts, London, England, 2012.
5. Richard Szeliski, "Computer Vision – Algorithms and Applications", Springer – Verlag London Limited, 2011.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	2	2	2	1	1	1
CO2	2	2	2	1	1	1
CO3	2	2	2	1	1	1
CO4	3	3	3	3	3	2
CO5	3	3	3	3	3	2
AVG	12/5=2.4	12/5=2.4	12/5=2.4	9/5=1.8	9/5=1.8	7/5=1.4

VE3204 VLSI SIGNAL PROCESSING TECHNIQUES L T P C
3 0 0 3

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING FOR FIR FILTERS 9

Overview of Discrete Time signal processing systems – FPGA Technology- DSP Technology Requirements- Data flow and Dependence graphs - Critical path, Loop bound, Iteration bound, Longest path matrix Algorithm, Pipelining and Parallel Processing of FIR filters.

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UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – Parallel FIR filter - Fast FIR algorithms - Parallel Architectures for Rank-order filters - Odd-Even merge-sort architecture, parallel rank-order filters

UNIT III FAST CONVOLUTION, PIPELINED AND PARALLEL RECURSIVE AND ADAPTIVE FILTERS 9

Fast convolution – Cook-Toom algorithms, Modified Cook Toom algorithm, Winograd algorithms, Pipelined and parallel recursive filters – Pipeline Interleaving in Digital Filters- Pipelining in I & II order Digital Filter – Parallel Processing for IIR Filter- Pipelined Adaptive Digital Filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers - Design of Lyon's bit-serial multipliers using Horner's rule, Bit-serial FIR filter design - CSD Arithmetic, CSD multiplication using Horner's rule for precision improvement - Distributed Arithmetic - Offset binary coding.

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Sub-expression Elimination, Multiple Constant Multiplication, Sub-expression sharing - Synchronous pipelining and Clocking styles - Clock skew in edge-triggered single phase clocking and Two-phase clocking - Wave Pipelining - NPCPL - Asynchronous Pipelining.

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the critical path of the DSP architectures
CO2: Design efficient retiming architecture for FIR filter using data flow graphs
CO3: Analyze various bit-level arithmetic architectures used in signal processing applications
CO4: Design fast convolution algorithms to minimize computational complexity
CO5: Analyze and implement proper clocking techniques on VLSI circuits

REFERENCES:

1. Roger Woods, John McAllister, Gaye Lightbody and Ying Yi, "FPGA-based Implementation of Signal and Data Processing Systems**",** Wiley, 2017.
2. U. Meyer Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2013.
3. Shoab Ahmed Khan, "Digital Design of Signal Processing Systems - A Practical Approach", A John Wiley and Sons, Ltd., Publication, 2011.
4. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
5. Lars Wanhammar, "DSP Integrated Circuits", Academic Press, 1999

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	3	3	2	1
CO2	3	1	3	3	2	1
CO3	3	1	3	3	2	1

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CO4	3	1	3	3	2	1
CO5	3	1	3	3	2	1
AVG	15/5=3	5/5=1	15/5=3	15/5=3	10/5=2	5/5=1

VE3205 EMBEDDED AUTOMATION L T P C
3 0 2 4

UNIT I AVR ATMEGA2560 MICROCONTROLLER 9+6

Features – Architecture – Memory Organization – System Clock and Clock Options - Power Management and Sleep Modes - System Control and Reset - I/O Ports – Timers/Counters – 8-bit Timer/Counter with PWM - Interrupts – ADC – Output Compare Modulator - SPI – USART – Two Wire Interface - Analog Comparator - JTAG Interface and On-chip Debug System - Boot Loader Support - System Development Tools.

UNIT II PERIPHERAL INTERFACING WITH AVR 9+6

Lights and Switches - Stack operation - Implementing Combinational Logic - Serial Port - Expanding I/O - Interfacing ADC and DACs - LED - Seven Segment Display - Dot matrix Display - LCD - Sensors - Keypad - Relays - Stepper Motor - Servo Motor - EEPROM - Real Time Clock - Accessing a Constant Table - Arbitrary Waveform Generator - Implementing a Finite State Machine - Generating Random Numbers

UNIT III AVR COMMUNICATION LINKS AND INTERNET OF THINGS 9+6

RS232 - RS422/423 - RS485 - SPI and Microwire Bus - I2C - PC Parallel Port - ISA Bus - USB - IrDA Data Link - CAN Bus - Ethernet - Bluetooth - ZigBEE - WiFi - Internet of Things - Definition - IoT Device Components - IoT Layers - IoT Deployment Levels - IoT Applications.

UNIT IV PCB DESIGN AND SIMPLE AUTOMATION PROJECTS 9+6

PCB - Schematic Symbol, Capture, Properties and Generation - Circuit Board Placement and Routing Considerations - Fabrication Methods and Guidelines - Testing and Verification - Proximity sensor/RFID/GSM based Door Open/Close system - Password Authenticated Door Lock - Smart Mailbox - Curtain Automation - Package Delivery Detector - Temperature controlled Incubator.

UNIT V ADVANCED EMBEDDED AUTOMATION PROJECTS 9+6

Smart Home Automation System - Web/Android controlled Light - Automated Bottling Plant - Automation of Water tank - Automated Garage Open/Close System - Automated Irrigation System - Elevator Design - Vision based Unauthentic Entry Identifier - Automated Guided Vehicle.

LIST OF EXPERIMENTS:

1. Water level controller
2. Unauthorized entry identifier
3. Tweeting bird feeder
4. Package delivery detector
5. Web enabled light switch
6. Curtain automation
7. Android door lock
8. Voice controlled home automation
9. Smart Lighting
10. Smart Mailbox

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11. Proximity garage door opener

TOTAL: 45 +30 = 75 PERIODS

COURSE OUTCOMES:

CO1: To be able to explain the features and functionalities of different blocks in an architecture of AVR ATMEGA2560 MCU .

CO2: To be able to configure and program the peripherals connected to ATMEGA2560 MCU.

CO3: To be able to transfer (transmit/receive) data through wired or wireless mode from AVR microcontroller.

CO4: To be able to design and develop automation systems using Embedded C programming.

CO5: To be able to apply the design skill in building simple and advanced embedded automation systems.

REFERENCES:

1. Muhammad Ali Mazidi, Sepehr Naimi and Sarmad Naimi, “The AVR Microcontroller and Embedded Systems using Assembly and C - Using Arduino Uno and Atmel Studio”, Pearson Education India, 2013.
2. Mike Riley, “Programming your Home - Automate with Arduino, Android and your Computer”, The Pragmatic Programmers, LLC, 2012.
3. Steven F. Barrett, Daniel J. Pack, “Atmel AVR Microcontroller Primer - Programming and Interfacing”, Morgan and Claypool Publishers, 2008.
4. Jon Varteresian, “Fabricating Printed Circuit Boards”, Newnes Publication - Elsevier, 2002.
5. Dhananjay V. Gadre, “Programming and Customizing the AVR Microcontroller”, McGraw-Hill, 2001.

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CO2	1	2	2	1	1	1
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CO5	3	3	3	3	3	2
AVG	9/5=1.8	12/5=2.4	11/5=2.2	9/5=1.8	8/5=1.6	6/5=1.2

VE3211 **ANALOG SYSTEM DESIGN LABORATORY** **L T P C**
0 0 4 2

PART I MODULE DESIGN AND SIMULATION USING ANALOG DESIGN ENVIRONMENT

1. Design of Common Source amplifier
2. Design of Common Drain amplifier
3. Design of Cascade amplifier
4. Design of Floded Cascode amplifier
5. Design of two-stage operational amplifier
6. Design of differential pair amplifier
7. Design of telescopic amplifier circuit
8. Design of current Mirrors

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PART II LAYOUT EXTRACTION AND SIMULATION USING ANALOG DESIGN ENVIRONMENT

9. Layout generation, parasitic extraction and layout simulation for experiments 1 to 3.

PART III ANALOG BLOCK HARDWARE DESIGN USING FPAA

10. Design of variable gain amplifier
11. Design of Full wave Rectifier
12. Design of Voltage Control Oscillator
13. Design of PD Controller
14. Design of PI Controller
15. Filtering Audio signal from noises using notch filter
16. Analyzing frequency response of Band pass filter
17. Monitoring Heart rate signal using PPG sensor

TOTAL: 60 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design basic and advanced analog circuits
CO2: Design and simulate various amplifiers
CO3: Import the standard cells in analog domain
CO4: Synthesize Place and Route the analog ICs
CO5:Design and analyze various analog blocks using FPAA

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	3	3	3	1	2
CO2	3	3	3	3	2	2
CO3	3	2	3	3	2	2
CO4	3	2	3	3	2	2
CO5	3	2	3	3	2	2
AVG	15/5=3	12/5=2.4	15/5=3	15/5=3	9/5=1.8	10/5=2

VL3051 ASIC DESIGN L T P C
3 0 0 3

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICS WITH LOGIC CELLS AND I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECUTRE 9

Architecture and configuration of Artix / Cyclone and Kintex Ultra Scale / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING 9

Logic synthesis - Floor Planning Goals and Objectives, Measurement of Delay in floor planning,

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Floor planning tools ,I/O and Power planning, Clock planning, Placement Algorithms. Routing: Global routing, Detailed routing, Special routing.

UNIT V SYSTEM-ON-CHIP DESIGN 9

SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High performance filters using delta-sigma modulators.
Case Studies: Digital camera, SDRAM, High speed data standards.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to apply logical effort technique for predicting delay, delay minimization and FPGA architectures
CO2: Ability to design logic cells and I/O cells
CO3: Ability to analyze the various resources of recent FPGAs
CO4: Ability to use algorithms for floorplanning and placement of cells and to apply routing algorithms for optimization of length and speed.
CO5: Ability to analyze high performance algorithms available for ASICs

REFERENCES:

1. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson, 2003.
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science, August 2007.
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation ofSignal Processing Systems”, Wiley, 2nd Edition, April 2017.
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill, 1994.
5. Douglas J. Smith, “HDL Chip Design”, Madison, AL, USA: Doone Publications, 1996.
6. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994
7. S.Pasricha and N.Dutt, “On-Chip Communication Architectures System on Chip Interconnect”, Elsveir, 2008.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	1			2	1	
CO2	2		2	2	1	
CO3	1			2	1	
CO4	3		3	3	1	
CO5		1		2	1	

VE3051 REAL TIME SYSTEMS L T P C
3 0 0 3

UNIT I EMBEDDED DESIGN PROCESS AND HARDWARE COMPONENTS 9

Complex Systems and RISC processors - Embedded System Design Process - Formalism for System Design - CPU - CPU Bus- CPU performance-CPU Power Consumption - Memory System Mechanism–Configuring and Programming Input and Output Peripherals - Supervisor Mode, Exceptions and Traps -Coprocessors.

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UNIT II SOFTWARE TOOLS AND EMBEDDED C PROGRAMMING 9

Compilation process - Native vs Cross-Compilers - Run-time libraries - Writing a library - Using Standard and alternative libraries - Porting Kernels –Techniques for Emulation and Debugging – Embedded C Program Structure– Data types - Operators, expressions and control statements – Functions and Procedures -Structures and union.

UNIT III ARM PROCESSOR 9

ARM features and architecture–Development Tools–ARM Instruction set-Thumb Instruction set– Architectural Support for System Development and operating systems

UNIT IV REAL TIME OPERATING SYSTEM 9

Concurrent Software – Foreground/Background systems, Multithreaded Programming, Shared resources and Critical sections – Scheduling – Cyclic, Round-Robin, Priority based, Deadline driven and Rate Monotonic schedules – Memory Management – Shared Memory -Commercial operating systems.

UNIT V EMBEDDED SYSTEM DESIGN, MODELING AND VERIFICATION 9

Finite State Machines - Moore Machine - Mealy Machine - Nondeterministic Finite Automation - Programming - UML State Machines - Petri Net Definition -Properties - Timed Petri Nets - Model Checking-Temporal Logic-NuSMV Model Checking Tool-Real Time Computation Tree Logic-Practical Issues.

TOTAL:45 PERIODS

COURSE OUTCOMES:

CO1: To be able to explain about different hardware components and software development tools.
CO2:To be able to describe the features, architecture and instruction set of ARM processor.
CO3: To be able to detail the concept and usage of RTOS in Embedded applications.
CO4:To be able to apply the embedded system design process while building real-time applications.
CO5:To be able to design a real time embedded system.

REFERENCES:

1. Daniel W. Lewis,"Fundamentals of Embedded Software with the ARM Cortex-M3",Pearson education limited,2nd Edition,2015.
2. Wayne Wolf,"Computers as Components-Principles of Embedded Computing System Design", Morgan Kaufmann Publishers,2nd Edition,June2008.
3. Andrew N.Sloss, Dominic Symes, Chris Wright,"ARM System Developer's Guide-Designing and Optimizing System Software",Morgan Kaufmann Publishers,2004.
4. Steve Heath, "Embedded Systems Design",Newnes Publications,2nd Edition,2003.
5. Steve Furber, “ARM system on chip architecture”, Pearson education limited, 2000

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	1	3	3	1	1	1
CO2	1	3	3	1	1	1
CO3	1	3	3	1	1	1
CO4	3	2	3	3	3	1
CO5	3	2	3	3	3	1
AVG	9/5=1.8	13/5=2.6	15/5=3	9/5=1.8	9/5=1.8	5/5=1

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VE3001 REAL TIME OPERATING SYSTEMS L T P C
3 0 0 3

UNIT I REAL TIME EMBEDDED SYSTEMS 9

Introduction - Classification of Real time systems and Embedded systems - Real time services and standards - System resources - Analysis - Service utility - Scheduling Classes - Cyclic executive - Scheduler concepts- Real time operating System - Thread safe Reentrant Functions

UNIT II RESOURCES AND SERVICES 9

Processing - Resources - Memory – Multi resource services : Blocking, Deadlock, livelock, Critical sections to protect shared resources, Priority inversion, Power management and Processor clock modulation - Soft real time services : Missed deadlines, Quality of Service, Alternatives to Rate monotonic policy, Mixed hard and soft real time services.

UNIT III REAL TIME EMBEDDED COMPONENTS 9

Hardware components - Firmware components - RTOS system software - Software application components - Traditional Hard real time operating systems : Asymmetric Multicore Processing and Symmetric Multi-core Processing - Processor core affinity - SMP support models - RTOS Hypervisors- Open source real time operating systems

UNIT IV INTEGRATING EMBEDDED LINUX 9

Integrating Embedded Linux into Real time systems - Debugging Components - Performance tuning - High availability and Reliability Design - Hierarchical approaches for fail-safe design

UNIT V CASE STUDIES 9

System life cycle – Healthcare - Continuous Media applications - video and audio processing - Robotic applications- Computer vision applications

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Complete understanding of scheduling algorithm and process
CO2: Better understanding on firmware and tools related to the development of RTOS
CO3: To be able to design and develop an embedded system with RTOS functionality
CO4: To be able to design and develop the systems in Linux environments
CO5: To be able to develop large real-time embedded systems

REFERENCES:

1. Wang K.C., “Embedded and Real Time Operating System”, Springer, 2017
2. Jonathan W. Valvano, "Embedded Systems: Real time operating systems for ARM Cortex-M Microcontrollers", Createspace Independent Publishing Platform, Fourth Edition, 2017
3. Sam Siewert, John Pratt, "Real-time embedded components and systems with Linux and RTOS", Mercury Learning and Information LLC, 2016.
4. Tanenbaum, Andrew, “Modern Operating Systems”, 4th edition, Pearson Prentice Hall, USA, 2015.
5. Ivan CibrarioBertolotti, Politecnico di Torino and Gabriele Manduchi, Real-Time Embedded Systems: Open-Source Operating Systems Perspective,1 st edition, CRC Press,2012.
6. Giorgio C. Buttazzo, "Hard Real-Time Computing Systems - Predictable Scheduling Algorithms and Applications", Springer Science+Buisness Media, LLC, Third Edition, 2011.
7. Albert M. K. Cheng, "Real-Time Systems - Scheduling, Analysis and Verification", A John Wiley & Sons INC Publication, 2002.

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	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	3	3	1	3
CO2	3	1	3	3	3	1
CO3	3	1	3	3	3	1
CO4	3	1	3	1	3	1
CO5	3	1	3	3	2	3
AVG	15/5=3	5/5=1	15/5=3	13/5=2.6	12/5=2.4	9/5=1.8

NE3053 DIGITAL IMAGE AND VIDEO PROCESSING L T P C
3 0 0 3

UNIT I IMAGE ENHANCEMENT 9

Digital image fundamentals - Image sampling - Quantization - Spatial domain filtering- intensity transformations - Contrast stretching - Histogram equalization - Smoothing filters, Sharpening filters -Noise distributions-Meanfilters-Order statistics filter

UNIT II IMAGE TRANSFORMS 9

1DDFT-2DTransforms-DFT-DCT-Walsh-Hadamard-Slant-Haar-KLT-SVD-Wavelet transform

UNIT III IMAGE RESTORATION AND SEGMENTATION 9

Image restoration-degradation model-Unconstrained and Constrained restoration–Inverse filtering-Wiener filtering-Image segmentation-Thresholding-Edge detection-Edge linking-Region based methods-Texture Descriptors- Boundary Descriptors-Graph based segmentation - Hybrid methods

UNIT IV IMAGE COMPRESSION 9

Need for data compression -Redundancy-Image Compression Schemes-Run Length coding-Huffman - Arithmetic coding - LZW technique - Vector Quantization -JPEG—MPEG

UNIT V VIDEO PROCESSING 9

Sampling and Interpolation of video- Back ground Subtraction –Frame difference- Static and dynamic background modeling -Video analytics - Video object Segmentation - Object Detection - Face Recognition -Motion Estimation-Shadow removal.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On completion of the course the student should be able to

- **CO 1.** Implement image enhancement algorithms
- **CO 2.** Apply image transform for different imaging modalities
- **CO 3.** Perform different segmentation and restoration processes
- **CO 4.** Implement different compression techniques
- **CO 5.** Develop algorithms for computer vision problems

REFERENCES:

1. Rafael C. Gonzalez, Richard E. Woods, “Digital Image Processing”, Pearson Education, Inc.,4thEdition,2017
2. AnilK. Jain,"Fundamentals of Digital Image Processing”,Prentice Hall of India, 2015.
3. Richard Szeliski, "Computer Vision - Algorithms and Applications", Springer Verlag London Limited,2011.
4. Alan Bovik, “Handbook of Image and Video Processing”,2nd Edition, 2005.

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5. Milan Sonka, Vaclav Hlavac and Roger Boyle, “Image Processing, Analysis & Machine Vision”,Brookes/Cole,Vikas Publishing House, 2nd edition,1999.
6. Sid Ahmed, M.A., “ Image Processing Theory, Algorithms and Architectures”,Mc Graw Hill,1995.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	3	2	1	3
CO2	3	1	3	2	2	1
CO3	3	1	3	1	2	1
CO4	3	1	3	2	2	3
CO5	3	1	3	1	1	3
AVG	15/5=3	5/5=1	15/5=3	8/5=1.6	8/5=1.6	11/5=2.2

VE3002 MICRO ELECTRO MECHANICAL SYSTEMS AND MICROSYSTEMS L T P C
3 0 0 3

UNIT I INTRODUCTION TO MEMS 9

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II MICROMECHANICS 9

Elasticity, Stress, strain and material properties, Bending of thin films, Spring configurations, torsion deflection, Mechanical vibration, Resonance, Thermo mechanics - actuators, force and response time,Fracture and thin film mechanics

UNIT III MICRO ACTUATORS 9

Electrostatics: basic theory, electrostatic instability. Surface tension, Gap and finger pull up, Electrostatic actuators, comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators, bistable actuators.

UNIT IV INTERFACING AND PACKAGING 9

Electronic Interfaces, Feedback systems, Noise, Packaging: Dicing-Wafer level Packaging-Wafer bonding-Connections between layers-self assembly-higher level of packaging.

UNIT V CASE STUDIES 9

Optical MEMS, RF MEMS- System design basics, Case studies: Capacitive accelerometer, Peizo electric pressure sensor, MEMS scanners, Capacitive RF MEMS switch, performance issues.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the working of MEMS and Microsystems components
CO2: Analyze the principles of micro mechanism
CO3: Design and analyze the interfacing of MEMS and microsystems
CO4: Design the MEMS accelerometer and to design Electrostatic actuators
CO5: Analyze the working of RF and Optical MEMS

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REFERENCES:

1. Eun Sokm Kim “Fundamentals of Micro electro mechanical Systems (MEMS)” McGraw Hill Professional, 2021
2. Stephen D Senturia, “Microsystems Design”, 2nd edition Springer Publishers, 2013.
3. Ville Kaajakarrai, “ Practical MEMS”,Small Gear Pub., 2009
4. Tai - Ran Hsu, “MEMS and Micro Systems: Design, Manufacture and Nano scale Engineering”, 2nd Edition, Tata McGraw Hill, New Delhi, 2008.
5. Mohamed Gad-el-Hak, Editor, “The MEMS Handbook”, 2nd Edition, CRC press, 2005.
6. Nadim Maluf and Kirt Williams, “Introduction to Micro electro mechanical Systems Engineering”, Artech House, 2004.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	1	1	3	2	1	1
CO2	1	1	3	2	1	1
CO3	1	2	3	2	1	1
CO4	1	2	3	2	1	1
CO5	1	1	3	1	3	1
AVG	5/5=1	7/5=1.4	15/5=3	9/5=1.8	7/5=1.4	5/5=1

NE3251 ADAPTIVE SIGNAL PROCESSING TECHNIQUES L T P C
3 0 0 3

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 9

Discrete Random Processes, Random variables, Parseval's theorem, Wiener Khintchine relation,Power Spectral Density, Spectral factorization, Filtering Random Processes, Special types of Random Processes

UNIT II SPECTRAL ESTIMATION 9

Introduction, Non parametric methods – Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric methods – ARMA, AR and MA model based spectral estimation, Solution using Levinson-Durbin algorithm.

UNIT III WEINER AND ADAPTIVE FILTERS 9

Weiner Filter: FIR wiener filter, IIR wiener filter, Adaptive Filter: FIR adaptive filters – Steepest descent method- LMS algorithm, RLS adaptive algorithm, Applications.

UNIT IV DETECTION AND ESTIMATION 9

Bayes detection techniques, MAP, ML – detection of M-ary signals, Neyman Peason, minimax decision criteria. kalman filter- Discrete kalman filter, The Extended kalman filter, Application.

UNIT V SYNCHRONIZATION 9

Signal parameter estimation, carrier phase estimation, symbol timing estimator, joint estimation of carrier phase and symbol timing.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1 Analyze the basic principles of discrete random signal processing.

CO2 Analyze the principles of spectral estimation.

CO3 Analyze and design the Weiner and adaptive filters.

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CO4 Analyze the different signal detection and estimation methods.
CO5 Design the synchronization methods for proper functioning of the system

REFERENCES:

1. John G. Proakis., "Digital Communication", McGraw Hill Publication, 5th edition,2014.
2. Simon Haykin, “Adaptive Filter Theory”, Pearson Education, 5th edition,2013.
3. Paulo S. R. Diniz, “Adaptive Filtering Algorithms and Practical Implementation”, Springer,4th edition,2013.
4. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley andSons, Inc, Singapore ,2009.
5. Kay Steven M, “Fundamentals of Statistical Processing: Estimation Theory Volume 1 and 2 (Estimation & detection Theory”, Pearson,1993 .

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	2	2	1	1
CO2	3	1	2	2	1	1
CO3	3	1	2	2	1	1
CO4	3	1	2	2	1	2
CO5	3	1	2	2	1	2
AVG	15/5=3	5/5=1	10/5=2	10/5=2	5/5=1	7/5=1.4

VE3003 VLSI FOR WIRELESS COMMUNICATION L T P C
3 0 0 3

UNIT I COMMUNICATION CONCEPTS 9

Introduction – Overview of Wireless systems – Standards – Access Methods – Modulation schemes – Classical channel – Wireless channel description – Path loss – Multipath fading.

UNIT II TRANSMITTER AND RECEIVER ARCHITECTURES 9

VLSI Model for Transmitter back end design – Quadrature LO generator, VLSI Model for Receiver front end – Filter design – Non- idealities – Design parameters – Noise figure & Input intercept point. CMOS LNA Introduction – Wideband LNA design – Narrow band LNA design: Impedance matching & Core amplifier.

UNIT III CMOS MIXERS 9

CMOS Active Mixer: Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Noise - A Complete Active Mixer.

CMOS Passive Mixer: Switching Mixer – Distortion, Conversion Gain & Noise in Unbalanced Switching Mixer- A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain, Distortion, Intrinsic & Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV ANALOG TO DIGITAL CONVERTERS 9

VLSI implementation: Demodulators – A/D converters used in receivers – Low-pass and band-pass sigma delta modulators and its implementation-I/Q mismatch in converters

UNIT V FREQUENCY SYNTHESIZERS 9

CMOS based PLL – Phase detector – Dividers – Voltage Controlled Oscillators – LC oscillators – Ring Oscillators – Phase noise – Loop filters & design approaches – A complete synthesizer design example (DECT).

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TOTAL: 45 PERIODS

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COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Apply the VLSI concepts in wireless communication techniques
CO2: Design and analyze the LNA and Mixers
CO3: Design and analyze PLL for real time applications
CO4: Analyze the characteristics of receivers and frequency synthesizers
CO5: Design and analyze A/D converters

REFERENCES:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" ,2nd Edition, McGraw-Hill, 2017.
2. Bosco H Leung "VLSI for Wireless Communication", Second Edition, Springer, 2014.
3. B.Razavi ,"RF Microelectronics" , Pearson ,2013.
4. J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, Kluwer Academic Pub., 2013.
5. Rappaport,T.S., "Wireless communications", Pearson Education, 3rd Edition, 2010.
6. Thomas H.Lee, "The Design of CMOS Radio – Frequency Integrated Circuits", Cambridge University Press ,2004.
7. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI wireless design – Circuits & Systems", Kluwer Academic Publishers, 2000.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	3	2	2	1
CO2	3	1	3	2	2	1
CO3	3	1	3	2	2	1
CO4	3	1	3	2	2	1
CO5	3	1	3	2	2	1
AVG	15/5=3	5/5=1	15/5=3	10/5=2	10/5=2	5/5=1

VE3004 COMPUTER AIDED DESIGN FOR VLSI SYSTEMS L T P C
3 0 0 3

UNIT I VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of VLSI Design automation tools –Graph theory and computational complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II LAYOUT COMPACTION, PLACEMENT AND PARTITIONING 9

Design rules –Symbolic layout - Problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation –wire length estimation –types of placement problem - Placement algorithms –partitioning

UNIT III FLOOR PLANNING AND ROUTING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - Global routing: introduction and algorithms.

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UNIT IV SIMULATION AND LOGIC SYNTHESIS 9

Gate level modeling and simulation –Switch level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V HIGH LEVEL SYNTHESIS 9

Hardware models - Internal representation of input algorithms –Allocation - Assignment - scheduling–scheduling algorithms - assignment problems - high level transformations.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Implement, simulate and synthesis the computer aided design of VLSI systems
CO2: Analyze the Algorithmic Graph Theory and computational complexity optimization
CO3: Analyze the concepts of layout design rules and floor planning
CO4: Design and optimize circuits using various graphical algorithms
CO5: Simulate and synthesis different hardware models

REFERENCES:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2013.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, Reprint - 2008.
3. Sadiq M Sait, Habib Youssef Vlsi Physical Design Automation: Theory And Practice
4. World Scientific. 1999.
5. Christoph Meinel and Thorsten Theobald, "Algorithms and Data structures in VLSI Design - OBDD Foundations and Applications", Springer Verlag, Berlin Heidelberg, New York, 1998.
6. Shin-ichi Minato, "Binary Decision Diagrams And Applications for VLSI CAD", Kluwer Academic Publishers, First edition, 1996.
7. M. Sarrafzadeh and C. K. Wong, “An Introduction to VLSI Physical Design”, McGraw Hill, 1996.
8. Prithviraj Banerjee, "Parallel Algorithms for VLSI Computer-Aided Design", Prentice Hall Inc., 1994.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	2	1	2	1	1	2
CO2	3	1	2	1	2	1
CO3	3	1	1	1	2	1
CO4	2	1	2	3	1	1
CO5	2	1	2	1	1	1
AVG	12/5=2.4	5/5=1	9/5=1.8	7/5=1.4	7/5=1.4	6/5=1.2

VE3005 HARDWARE - SOFTWARE CO-DESIGN OF EMBEDDED SYSTEM L T P C
3 0 0 3

UNIT I NATURE OF HARDWARE AND SOFTWARE 9

Hardware, Software, Definition of Hardware/Software Co-Design – Driving factors Platform design space – Application mapping – Dualism of Hardware design and software design – Concurrency and parallelism, Data flow modeling and Transformation – Data Flow Graph – Tokens, actors and queues, Firing rates, firing rules and Schedules – Synchronous data flow

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graph – control flow modeling – Adding time and resources – Transformations.

UNIT II DATA FLOW IMPLEMENTATION IN SOFTWARE AND HARDWARE 9

Software Implementation of Data Flow – Converting queues and actors into software, Dynamic Scheduler – Hardware Implementation of Data Flow – single rate SDF graphs into hardware, Pipelining – Analysis of control flow and data flow – construction of control and data flow graph – Translating C into hardware – Designing data path and controller.

UNIT III DESIGN SPACE OF CUSTOM ARCHITECTURES 9

Finite state machines with datapath – FSMD design example, Limitations – Microprogrammed Architecture – Microprogrammed control, microinstruction encoding, Microprogrammed data path, microprogrammed machine – General purpose Embedded Core – RISC pipeline, Program organization – SoC interfaces for custom hardware – Design Principles in SoC Architecture

UNIT IV HARDWARE/ SOFTWARE INTERFACES 9

Principles of Hardware/software communication – synchronization schemes, communication constrained versus Computation constrained, Tight and Loose coupling - On-chip buses – Memory mapped interfaces – coprocessor interfaces – custom instruction interfaces – Coprocessor hardwareinterface – Data and control design, programmer's model.

UNIT V APPLICATIONS 9

Zynq processor-centric platforms-Scalable Processor Architecture, Trivium for 8-bit platforms – AEScoprocessor, CORDIC coprocessor – algorithm and implementation.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the key concepts in hardware/software co-design

CO2: Analyze the data flow implementation in software and hardware

CO3: Design the fundamental building blocks using hardware/software co-design and related implementation

CO4: Design and analyze with modern hardware/software tools for building prototypes of embeddedsystems

CO5: Analyze the various processors

REFERENCES:

1. Patrick Schaumont, "A Practical Introduction to Hardware/Software Co-design", 2nd Edition,Springer, 2014.
2. Louise H. Crockett, "Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 AllProgrammable SoC" Strathclyde Academic Media,2014
3. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub, 2013.
4. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems",Kluwer Academic Pub, 2010.
5. Giovanni De Micheli, Rolf Ernst Morgon, "Reading in Hardware/Software Co-Design" KaufmannPublishers, 2002.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	2	1	2	2	2	2
CO2	3	1	3	3	3	2
CO3	3	1	3	3	3	2
CO4	3	1	3	3	3	2
CO5	3	1	3	3	3	2
AVG	14/5=2.8	5/5=1	14/5=2.8	14/5=2.8	14/5=2.8	10/5=2

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VE3006 EMBEDDED NETWORKING L T P C
3 0 0 3

UNIT I COMMUNICATION PROTOCOLS 9

Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming – ISA/PCI Bus protocol.

UNIT II USB AND CAN BUS 9

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC Microcontroller USB Interface – CAN Bus– Introduction - Basic Concepts & Definitions-Identifiers & Arbitration-Robustness & Flexibility-Message Formats-Error Handling -PIC microcontroller CAN Interface –A simple application with CAN.

UNIT III ETHERNET BASICS 9

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT IV EMBEDDED ETHERNET 9

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP.

UNIT V EMBEDDED WIRELESS SENSOR NETWORKS 9

Wireless sensor networks –Introduction to WSN-Challenges for WSNs - Characteristic requirements - Single-node / Multi-node architecture -Hardware components-Energy consumption of sensor nodes-Operating systems and execution environments-Some examples of sensor nodes.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the wired and wireless network protocols

CO2: Design an application using embedded networking

CO3: Analyze the basics of Ethernet

CO4: Incorporate networks in embedded systems

CO5: Analyze the basics of wireless sensor networks

REFERENCES:

1. Dogan Ibrahim, “Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series” - Elsevier 2008.
2. Frank Vahid, Tony Givargis, “Embedded Systems Design: A Unified Hardware/Software Introduction” - John & Wiley Publications, 2006
3. Bhaskar Krishnamachari, Networking, Wireless Sensors - Cambridge press 2005.
4. Holgerkarl, Andreas Willig, “Protocols and architectures for wireless sensor networks”, John Wiley,2005.
5. Olaf Pfeiffer, Andrew Ayre and Christian Keydel, “Embedded Networking with CAN and CAN open”, Second edition published by Copperhill Media Corporation, 2003
6. Jan Axelson, “Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port” - Penram Publications, 1996.

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	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	2	1	2	3	1	3
CO2	2	1	3	3	3	1
CO3	2	1	2	3	1	1
CO4	3	1	3	1	3	1
CO5	2	1	2	3	1	1
AVG	11/5=2.2	5/5=1	12/5=2.4	13/5=2.6	9/5=1.8	7/5=1.4

VE3007 **QUANTUM COMPUTING** **L T P C**
3 0 0 3

UNIT I QUANTUM COMPUTATIONS AND ALGORITHMS 9

Introduction – signal states – logic operations – quantum measurement – integer factorization – order finding – phase and eigen value estimation - hidden subgroup problem – grover's and adiabatic algorithms.

UNIT II QUANTUM ARCHITECTURES AND SIMULATION 9

Reliable and realistic implementation technology – robust error correction and fault tolerant structures – quantum resource distribution – simulation of error propagation– stabilizer method.

UNIT III ARCHITECTURAL ELEMENTS AND PROGRAMMING 9

Processing elements – memory hierarchy – addressing schemes – architecture design – Quantum array logic architecture – Programming: physical level instruction scheduling – high level compiler design – architecture independent circuit synthesis – mapping – optimization.

UNIT IV REVERSIBLE LOGIC: FUNDAMENTALS AND SYNTHESIS 9

Reversible logic gates – synthesis – expansions and spectral transforms – garbage elimination decision trees and diagrams – lattice and fast transformation circuits – group theoretic representations – reconstructability analysis – reversible programmable gate array – evaluation.

UNIT V REVERSIBLE SEQUENTIAL LOGIC CIRCUITS 9

Reversible flip flops – complex reversible sequential circuits – novel reversible elements – multiple valued circuits.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the basics of quantum computing
CO2: Design and analyze quantum architectures and algorithms
CO3: Design and simulate the basic elements using quantum computing
CO4: Design reversible logic circuits
CO5: Design and analyze sequential circuits using reversible logic

REFERENCES:

1. Bernard Zygelman, "A First Introduction to Quantum Computing and Information" Springer 2018.
2. Aboul Ella Hassanien, Mohamed Elhoseny and Janusz Kacprzyk, "Quantum Computing: An Environment for Intelligent Large Scale Real Application" Springer 2018.
3. Saleem Mohammed RidhaTaha, "Reversible Logic Synthesis Methodologies with Application to Quantum Computing" Springer, 2016.

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4. Jennifer Chubb, Ali Eskandarian, Valentina Harizanov, “Logic and Algebraic Structures in Quantum Computing” Series: Lecture Notes in Logic, Cambridge University Press, 2016.
5. Tzvetan S. Metodi, Arvin I. Faruque and Frederic T. Chong, “Quantum Computing for Computer Architects” Second Edition, Morgan and Claypool Publishers, 2011.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	3	2	1	1
CO2	3	1	2	2	1	1
CO3	3	1	2	2	1	1
CO4	3	1	2	2	1	1
CO5	3	1	2	2	1	1
AVG	15/5=3	5/5=1	11/5=2.2	10/5=2	5/5=1	5/5=1

VE3008 MULTI-CORE ARCHITECTURES AND PROGRAMMING L T P C
3 0 0 3

UNIT I INTRODUCTION TO MULTIPROCESSORS AND SCALABILITY ISSUES 9

Scalable design principles – Principles of processor design – Instruction Level Parallelism, Thread level parallelism. Parallel computer models –- Symmetric and distributed shared memory architectures – Performance Issues – Multi-core Architectures - Software and hardware multithreading – SMT and CMP architectures – Design issues – Case studies – Intel Multi-core architecture – SUN CMP architecture.

UNIT II PARALLEL PROGRAMMING 9

Fundamental concepts – Designing for threads – scheduling - Threading and parallel programming constructs – Synchronization – Critical sections – Deadlock - Methods for handling deadlocks – Deadlock Prevention – Deadlock Avoidance – Deadlock detection – Recovery from deadlock - Threading APIs.

UNIT III OPENMP PROGRAMMING 9

OpenMP – Threading a loop – Thread overheads – Performance issues – Library functions. Solutions to parallel programming problems – Data races, deadlocks and livelocks – Non-blocking algorithms – Memory and cache related issues

UNIT IV MPI PROGRAMMING 9

MPI Model – collective communication – data decomposition – communicators and topologies – point-to-point communication – MPI Library.

UNIT V MULTICORE ARCHITECTURES FOR EMBEDDED SYSYETMS 9

Architectural Considerations, Interconnection Networks, Software Optimizations. Case Studies: HiBRID SoC for Multimedia Signal Processing, VIPER Multiprocesssor SoC, General Purpose Multiprocessor DSP, Multicore DSP Platforms.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the basics of multicore processing

CO2: Analyze the principles of parallel programming

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CO3: Analyze the principles of different multiprocessors with their performance issues
CO4: Analyze the fundamentals of various programming concepts used in multicore architectures
CO5: Design the concepts of multicore architectures for embedded systems

REFERENCES:

1. John L. Hennessey and David A. Patterson, " Computer architecture – A quantitative approach", Morgan Kaufmann/Elsevier Publishers, 4th. edition, 2017.
2. Gerassimos Barlas, "Multicore and GPU Programming: An Integrated Approach", Elsevier, 2014
3. Bryon Moyer, "Real world Multicore Embedded systems", Elsevier, 2013.
4. Georgios Kornaros, "Multicore Embedded systems", CRC Press, Taylor & Francis Group, 2010
5. Shameem Akhter and Jason Roberts, "Multi-core Programming", Intel Press, 2006.
6. Michael J Quinn, Parallel programming in C with MPI and OpenMP, Tata Mcgraw Hill, 2004.
7. Andrew S. Tanenbaum, "Modern Operating Systems", Addison Wesley, 2nd Edition, 2001.
8. David E. Culler, Jaswinder Pal Singh, "Parallel computing architecture : A hardware/ software approach" , Morgan Kaufmann/Elsevier Publishers, 2000.

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CO3	3	1	3	1	2	1
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CO5	3	1	2	1	2	1
AVG	15/5=3	5/5=1	12/5=2.4	5/5=1	10/5=2	5/5=1

WT3055 **RF IC DESIGN** **L T P C**
3 0 0 3

UNIT I COMPONENTS FOR RF IC **9**

Capacitance, Inductance, Circuit representations, Distributed and Lumped circuits,, LC and RLC circuits, Antennas, Integrated capacitors, Integrated inductors, plane waves, Antennas.

UNIT II LOW NOISE AMPLIFIERS **9**

Types of Noise, Two port Equivalent Noise, Noise figure, Minimum NF,Noise figure of cascade of stages, CS and CG LNA, series and shunt feedback LNA,, Feed forward LNA,s, LNA power noise optimization, LNA design case study

UNIT III POWER AMPLIFIER DESIGN **9**

Small and Large signal Non linearities, Class A, B, C, D, E and F amplifiers,, Class D Digital power amplifiers, Linearization Techniques, RF power amplifier design example.

UNIT IV PLL, FREQUENCY SYNTHESIZERS AND OSCILLATORS **9**

PLL basics, Type I – PLL, Type – II PLL, Integer N frequency synthesizers, Fractional N frequency Synthesizers, Frequency dividers, Digital PLLs. Ring oscillators, Quadrature Oscillators, Crystal and FBAR Oscillators

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UNIT V SYSTEM ARCHITECUTRE 9

Analog Linear modulation, non linear Modulation, Modern radio modulation, SSB receivers, Receiver architectures, Blocker tolerant receivers, Receiver filtering and AGC design, Transmitter architectures, Transceiver design considerations

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the RF integrated circuits
CO2: Design low noise amplifiers
CO3: Design power amplifiers
CO4: Design PLL and frequency synthesizers
CO5:Develop RF transceivers and its building blocks

REFERENCES:

1. Hooman Darabi," Radio Frequency Integrated Circuits and Systems", Cambridge University Press, Cambridge, 2020
2. Cam Nguyen," Radio frequency integrated circuit Engineering", John Wiley, New Jersy,2015.
3. Matthew M.Radmanesh "RF and Microwave Design Essentials", AuthorHouse, Bloomington,2007.
4. Thomas Lee, "The Design of Radio Frequency CMOS Integrated Circuits", Cambridge UniversityPress, 2nd Edition, Cambridge, 2004.
5. John W.M.Rogers and Calvin Plett, "Radio Frequency Integrated Circuit Design", 2nd Edition, Artech House, Norwood, 2010.

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CO3	3	1	3	2	2	1
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CO5	3	1	3	2	2	1
AVG	15/5=3	5/5=1	15/5=3	10/5=2	10/5=2	5/5=1

PROGRESS THROUGH KNOWLEDGE

VE3009 ADVANCED CMOS ANALOG IC DESIGN L T P C
3 0 0 3

UNIT I NOISE IN INTEGRATED CIRCUITS 9

Statistical Characteristics of Noise, Sources of noise, noise models of IC components, Circuit noise calculations, equivalent input noise generators, effect of feedback on noise performance, noise in CS,CD, CG and cascode amplifiers, noise in differential pair, noise bandwidth.

UNIT II OTA DESIGN CONSIDERATION 9

Step response, Slewing, OTA variations, CMFB implementation, Input resistance, Output resistance, Output Voltage swing, CMRR, PSRR of two-stage telescopic amplifiers.

UNIT III BANDGAP REFERENCE CIRCUIT AND SWITCHED CAPACITOR CIRCUITS 9

Supply Insensitive biasing, Temperature insensitive biasing, Sampling Switches, Speed

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Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers, Switched- Capacitor Integrator, Switched-Capacitor Common-Mode Feedback.

UNIT IV PERFORMANCE METRICS OF DATA CONVERTERS & NYQUIST RATE D/A CONVERTERS 9

Ideal Sampling, Reconstruction, Quantization, Static performance metrics, Dynamic performance metrics, Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs.

UNIT V ANALOG TO DIGITAL CONVERTERS 9

Single stage amplifier as comparator, resistor-based latched comparators. offset cancellation, Flash ADC, Successive approximation ADC, Pipelined ADC, Time Interleaved ADC.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design various analog block by considering noises and their effects

CO2: Design various OTA architectures and CMFB block

CO3: Design and analyze bandgap reference circuits

CO4: Analyze switched-capacitor circuits and the issue of non-linearity and mismatch in the circuits

CO5: Analyze data conversion circuits such as DAC and ADC and their design techniques

REFERENCES:

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Second Edition, Tata McGraw Hill, 2017.
2. Gray, Hurst, Lewis, Meyar, “Analysis and Design of Analog Integrated Circuits”, Fifth Edition John Wiley, 2016.
3. Phillip E.Allen, DouglasR.Holberg, “CMOS Analog Circuit Design”, Third edition, Oxford University Press, 2011.
4. Jacob Baker “CMOS: Circuit Design, Layout, and Simulation”, Third Edition, Wiley IEEE Press 2010
5. Rudy Van de Plassche, “CMOS Integrated ADC and DACs” 2nd Edition, Springer,2007

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AVG	15/5=3	5/5=1	15/5=3	8/5=1.6	8/5=1.6	5/5=1

VE3010 SoC DESIGN FOR EMBEDDED SYSTEM L T P C
3 0 0 3

UNIT I SYSTEM ARCHITECTURE: OVERVIEW 9

Components of the system – Processor architectures – Memory and addressing – system level

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interconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability

UNIT II PROCESSOR SELECTION FOR SOC 9

Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interrupts and exceptions. Basic elements in instruction handling –Minimizing pipeline delays – reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors,Processor Evolution.

UNIT III MEMORY DESIGN 9

SoC external memory, SoC internal memory, The size of memory–Scratch pads and cache memory – cache organization and write policies – strategies for line replacement at miss time – split I- and D- caches – multilevel caches – SoC memory systems – board based memory systems –memory array – simple processor/memory interaction.

UNIT IV INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION 9

Bus architectures – SoC standard buses – AMBA, Core Connect – Processor customization approaches – Reconfigurable technologies – mapping designs onto reconfigurable devices - FPGA based design – Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing.

UNIT V FPGA BASED EMBEDDED PROCESSOR 9

Hardware software task partitioning – FPGA fabric Immersed Processors – Soft Processors and Hard Processors – Tool flow for Hardware/Software Co-design –Interfacing Processor with memory and peripherals – Types of On-chip interfaces – Wishbone interface, Avalon Switch Matrix, OPB Bus Interface, Creating Customized Microcontroller - FPGA-based Signal Interfacing and Conditioning.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the components of a System-on-Chip and an embedded system
CO2: Analyze the major design flows for digital hardware and embedded software
CO3: Design and analyze the major architectures and trade-offs of chips and embedded systems
CO4: Design and analyze various interconnect architectures
CO5: Design memory circuits for embedded system applications

REFERENCES:

1. "Embedded Design Handbook - FPGA CPLD and ASIC", Intel, 2018
2. Michael J. Flynn and Wayne Luk**,** “Computer System Design: System-on-Chip”, John Wiley and sons, 2011.
3. Rahul Dubey, “Introduction to Embedded System Design Using Field Programmable Gate Arrays”, Springer Verlag London Ltd., 2009.
4. Sudeep Pasricha and Nikil Dutt, On-Chip Communication Architectures - System on Chip Interconnect”, Elsevier, 2008.
5. Michael Keating and Pierre Bricaud, "Reuse Methodology Manual for System -On-A-Chip Designs", Third Edition, Kluwer Academic Publishers, 2002.

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	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	2	2	1	1
CO2	3	1	2	2	1	1
CO3	3	1	2	2	1	1
CO4	3	1	3	2	1	1
CO5	3	1	3	2	1	1
AVG	15/5=3	5/5=1	12/5=2.4	10/5=2	5/5=1	5/5=1

VE3011 **ROBOTICS** **L T P C**
3 0 0 3

UNIT I INTRODUCTION **9**

Introduction, Rigid Transformation, Robot anatomy, Kinematics, Inverse Kinematics, Jacobians, Trajectory following, Statics and Dynamics.

UNIT II ARTIFICIAL LIFE AND ARTIFICIAL INTELLIGENCE **9**

History, Purpose of Robots, Artificial Intelligence, Artificial life- Nano robotics, Using neural networks in robots, Neural-Behavior based architecture.

UNIT III HARDWARE TOOLS **9**

Microcontrollers, Photovoltaic Cells, Fuel Cells, Batteries. Movement and Drive Systems- Air muscles, Nitinol wire, Solenoids, Rotary solenoids, Stepper motors, Servo Motors and DC motors. Sensors Signal conditioning, Light sensors, Machine vision, Body sense, Direction-magnetic fields, Speech recognition, Sound and ultrasonics, Touch and Pressure, Piezoelectric material, Switches, Bend sensors, Pressure sensor, Smell, Humidity, Testing sensor.

UNIT IV BASIC NAVIGATION **9**

Philosophies, Live Reckoning, The Best Laid Plans of Mice and Machines, Navigation as a filtering process, Hard navigation vs. Fuzzy navigation, Sensors, Navigation Agents and Arbitration, Instilling pain, Fear and Confidence, Becoming unstuck in Time, Programming Robots to be useful, Command, Control and Monitoring, The Law of Conservation of Defects and the Art of Debugging.

UNIT V DESIGN OF ROBOTS **9**

Telepresence robot, Mobile platforms, Walker Robots, Solar-ball Robot, Underwater bots, Aerobots, Robotic arm and IBM PC interface and speech control, Android hand.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the dynamics of robotics
CO2: understand the concepts of Artificial Intelligence in robotics
CO3: Analyze the hardware requirements for robotics
CO4: Design of navigation mechanisms involved in building a robotic system
CO5: To design the different types of robots

REFERENCES:

1. Bruno Siciliano, Lorenzo Sciavicco, Luigi Villani and Giuseppe Oriolo, "Robotics- Modeling, Planning and Control", Springer-Verlag London Limited 2010.
2. Robert J. Schiling, "Fundamentals of Robotics- Analysis and Control", Pearson Education,

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2006.
3. John M. Holland, "Designing Autonomous Mobile Robots-Inside the mind of an Intelligent Machine", Newnes Publication, 2004.
4. John Iovine, "Robots, Android and Animatronics", Second Edition, McGraw-Hill, 2002.
5. J. M. Selig, "Introductory Robotics", Prentice Hall, 1992.

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CO2	3	1	3	3	3	1
CO3	3	1	3	3	3	1
CO4	3	1	3	3	3	1
CO5	3	1	3	3	3	3
AVG	15/5 =3	5/5=1	15/5 =3	15/5 =3	15/5 =3	9/5=1.8

VE3012 EMBEDDED C PROGRAMMING L T P C
3 0 0 3

UNIT I INTRODUCTION 9

Basic concepts of C, Embedded C Vs C, Embedded programming aspects with respect to firmware and OS Functions- Data Variables and Types -Expression and Operators – Statements - Functions - Arrays - Structures - Memory and Pointers - Built in Functions – Strings - Function like Macros - Conditional Compilation

UNIT II 8-BIT MICROCONTROLLER 9

8-bit Microcontroller - Features - Architecture - Memory Organization - I/O Ports - Timers - Watchdog Timers - ADC - Interrupts - RESET - CCP Modules - USART - I2C - SPI - Parallel Slave Port

UNIT III CONFIGURATION AND PROGRAMMING 9

Minimal Hardware Connection - Device Programming - Hex Files - Power up Considerations - Clock Configuration - Integrated Development Environment -Debugging - Bootloading - Real Time Methods- Using Interrupts - State Machines

UNIT IV INTERFACING PERIPHERAL DEVICES 9

LED - LCD - Seven Segment Display - Motor (DC, Stepper, Servo) - Relay - Keypad - Keyboard - Sensors -, Global Positioning System - External Serial Buses - RS232 - RS422 - RS485 -USB - CAN – LIN

UNIT V RTOS PROGRAMMING & CASE STUDIES 9

Multitasking Operating Systems - Preemptive Scheduling - Dispatcher Scheduling - Deterministic Scheduling - Data and Resource protection - Semaphore - Message Passing - await () - Task management - Commercial operating systems - Linux - Disk partitioning - Tank Water Level Controller, Bank visitor counter - Digital Multimeter - Electronic Scooter

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design a system with embedded C programming and debugging skills

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CO2: Interface the peripheral device with microcontroller
CO3: Analyze the scheduling strategies, resource allocation and process methods involved in RTOS
CO4: Design and develop the hardware and software portion in Real-time embedded Systems
CO5: Design and develop innovative real time systems

REFERENCES:

1. Mark Siegesmund, "Embedded C Programming - Techniques and Applications of C and PIC MCUs", Newnes is an imprint of Elsevier, First Edition, 2014.
2. Robert Love, Linux System Programming: Talking directly to the kerneland C library: and C Library, 2013, 2nd Edition, O"Reilly Publication, USA.
3. Neil Mathew, Richard stones, Beginning Linux Programming, 2012 reprint, Wrox – Wiley Publishing, USA.
4. Tim Wilmshurst, "Designing Embedded Systems with PIC microcontrollers-Principles and Applications", Newnes Publications, 2007.
5. Muhammad Ali Mazidi, Rolin McKinlay, Danny Causey, "PIC Microcontroller and Embedded Systems: Using Assembly and C for PIC18", Prentice Hall publications, 2007.
6. Richard Barnett, Larry O'Cull, Sarah Cox, "Embedded C Programming with the Microchip PIC", Delmar Learning, a division of Thomson Learning, 2004.
7. Phillip A. Laplante, "Real-Time System Design and Analysis", A John Wiley & Sons, Inc, Third Edition, 2004.

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CO3	2	1	2	2	1	1
CO4	3	1	3	3	3	1
CO5	3	1	3	3	2	1
AVG	14/5=2.8	5/5=1	14/5=2.8	13/5=2.6	10/5=2	7/5=1.4

VE3013 DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES L T P C
3 0 0 3

UNIT I INTRODUCTION TO DIGITAL SIGNAL PROCESSING SYSTEMS 9

Fundamentals of DSP - Digital signal processor architectures – Software developments – Hardware issues – System considerations – Implementation considerations, Data representations, Finite word length effects, Programming issues, Real time implementation considerations.

UNIT II FIXED AND FLOATING POINT DIGITAL SIGNAL PROCESSORS 9

TMS320C55x – Architecture overview, Addressing modes, Instruction set, Programming considerations, system issues. TMS320C62x AND TMS320C64x - Architecture overview, Memory systems, External memory addressing, Instruction set, Programming considerations, system issues. TMS320C67X – Architecture overview, Instruction set, Pipeline Architecture, Programming considerations, Real time implementations.

UNIT III FAST FOURIER TRANSFORMS 9

Introduction to DFT – FFT algorithms – Decimation-in-time, Decimation-in-frequency - Fixed point implementation usingTMS320C64x, Floating point implementation using TMS320C67x.

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UNIT IV FIR AND IIR FILTER IMPLEMENTATIONS 9

FIR and IIR filters – Characteristics, Structures, FIR Filter design using Windowing and frequency sampling method, IIR Filter-Butterworth and Chebyshev Filter Design-, Fixed point implementation usingTMS320C64x, Floating point implementation using TMS320C67x.

UNIT V ADAPTIVE FILTER STRUCTURES AND ALGORITHMS 9

Wiener filter, LS filter , Filter structures, Adaptive algorithms, Properties and Applications – Fixed and floating point implementation using TMS320C64x and TMS320C67x.

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Develop the program for fixed and floating point DSP processors based on the design issues
CO2: Design and develop real time implementations on DSP algorithms
CO3: Design IIR and FIR filters with desired frequency responses
CO4: Apply the fast transforms for the analysis of DSP systems
CO5: Analyze the structures and algorithms of adaptive filters

REFERENCES:

1. Sen M.Kuo, Woon-Seng S.Gan, “Digital Signal Processors – Architectures, Implementations and Applications”, Pearson Education, 2005, Second Impression, 2009.
2. Lapsley et al “DSP Processor Fundamentals, Architectures & Features”, S.Chand & Co, 2000, Reprint.
3. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, Wiley, 2009.
4. John G Proakis and Manolakis, “Digital Signal Processing Principles, Algorithms and Applications”, Pearson, Fourth Edition, 2007.
5. TMS Manual on TMS320C64XX and TMS320C67XX.
6. A.V. Oppenheim, R.W.Schafer and J.R.Buck, "Discrete Time Signal Processing", Pearson, 2004.
7. S.K. Mitra, “Digital Signal Processing, A Computer Based approach", Tata McGraw-Hill,2006.
8. P. Vaidyanathan, “Multirate Systems & Filter Banks", Prentice Hall, 1993.
9. I.C.Ifeachor and B.W. Jervis, “Digital Signal Processing-A Practical Approach”, Pearson, 2002.

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CO5	3	1	3	3	2	1
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VE3014 RECONFIGURABLE ARCHITECTURES AND APPLICATIONS L T P C
3 0 0 3

UNIT I INTRODUCTION 9

General purpose computing – domain specific processors – application specific processors – reconfigurable computing – fields of application – evolution of reconfigurable systems – simple programmable logic devices – complex programmable logic devices – field programmable gate

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arrays – coarse grained reconfigurable devices.

UNIT II IMPLEMENTATION, SYNTHESIS AND PLACEMENT 9

Integration – FPGA design flow – Logic synthesis – LUT based technology mapping – modeling – temporal partitioning algorithms – offline and online temporal placement – managing device's free and occupied spaces.

UNIT III COMMUNICATION AND SoPC 9

Direct communication – communication over third party – bus based communication – circuit switching – network on chip – dynamic network on chip – system on a programmable chip – adaptive multi-processing on chip.

UNIT IV RECONFIGURATION MANAGEMENT 9

Reconfiguration – configuration architectures – managing the reconfiguration process – reducing configuration transfer time – configuration security.

UNIT V APPLICATIONS 9

FPGA based parallel pattern matching - Low power FPGA based architecture for microphone arrays in wireless sensor networks - Exploiting partial reconfiguration on a dynamic coarse grained reconfigurable architecture – Parallel pipelined OFDM baseband modulator with dynamic frequency scaling for 5G systems– Distributed Arithmetic– Software Defined Radio

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the different architecture principles relevant to reconfigurable computing systems

CO2: Compare the tradeoffs that are necessary to meet the area, power and timing criteria of reconfigurable systems

CO3: Analyze the algorithms related to placement and partitioning

CO4: Analyze the communication techniques and system on programmable chip for reconfigurable architectures

CO5: Analyze the principles of network and system on a programmable chip

REFERENCES:

1. Nikoloas Voros et al. "Applied Reconfigurable Computing: Architectures, Tools and Applications" Springer, 2018.
2. Scott Hauck and Andre Dehon, "Reconfigurable Computing: The Theory and Practice of FPGA based Computation", Elsevier 2008.
3. Christophe Bobda, "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications", Springer 2007.
4. Koen Bertels, João M.P. Cardoso, Stamatis Vassiliadis, "Reconfigurable Computing: Architectures and Applications", Springer 2006.
5. M. Gokhale and P. Graham, "Reconfigurable Computing: Accelerating Computation with FieldProgrammable Gate Arrays", Springer, 2005.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	3	2	1	1
CO2	3	1	3	2	1	1
CO3	3	1	2	1	2	1
CO4	3	1	3	1	2	1
CO5	3	1	3	1	2	1
AVG	15/5=3	5/5=1	14/5=2.8	7/5=1.4	8/5=1.6	5/5=1

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WT3053 PATTERN RECOGNITION AND MACHINE LEARNING L T P C
3 0 0 3

UNIT I BASICS OF PROBABILITY AND RANDOM PROCESS 9

Probability Theory - Conditional and Joint Probability - Expectation - Auto correlation - Cross Correlation - Eigen values - Eigen vectors - Decision Theory.

UNIT II DIMENSIONALITY REDUCTION 9

Introduction - Features, feature vectors - Feature selection and ranking - Discriminant functions - Fisher's Discriminant analysis - Principal Component Analysis - Independent component analysis

UNIT III LEARNING MODEL 9

Linear models for Classification and Regression - Classifiers based on Bayes Decision theory – Naïve Bayes - Nearest neighbor rules - Mixture models - Mixture of Gaussian - Hidden Markov Model

UNIT IV ARTIFICIAL NEURAL NEWORK 9

Supervised Learning - Unsupervised Learning- Reinforcement Learning – Feed Forward and Feedback architectures - Multilayer Perceptron - Back propagation Algorithm- Radial Basis Function networks - Support vector Machines

UNIT V DEEP LEARNING NETWORKS 9

Introduction to Deep neural networks – Convolution neural networks – Deep Belief Networks - Recurrent neural networks- case studies

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Employ different feature extraction and dimensionality reduction techniques
CO2: Design different learning models
CO3: Implement different neural network architectures
CO4: Realize basic Deep neural network architectures
CO5: Test and implement deep generative models for various data processing applications

REFERENCES:

1. Richard Szeliski, "Computer Vision - Algorithms and Applications", Springer Verlag London Limited, 2nd Edition, 2022.
2. Ethem Alpaydm, "Introduction to Machine Learning", The MIT Press, Cambridge, Fourth Edition, 2020.
3. Josh Patterson and Adam Gibson, "Deep Learning - A Practitioner's Approach", O'Reilly Media, Inc, 2017.
4. Kevin P. Murphy, "Machine Learning - A Probabilistic Perspective", The MIT Press, Cambridge, 2012.
5. Christopher M. Bishop,"Pattern Recognition and Machine Learning", Springer, 2011.
6. R.O. Duda, P.E. Hart and D.G. Stork, "Pattern Classification" John Wiley,2nd Edition, 2007.

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	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	1	1	1	2	2	2
CO2	1	1	1	2	1	1
CO3	2	1	1	2	3	3
CO4	3	2	2	2	3	3
CO5	3	2	2	2	3	3
AVG	10/5=2	7/5=1.4	7/5=1.4	10/5=2	12/5=2.4	12/5=2.4

VE3015 **ENERGY EFFICIENT VLSI DESIGN** **L T P C**
3 0 0 3

UNIT I POWER CONSUMPTION IN CMOS **9**

Introduction to MOS Devices- Hierarchy of limits of power –Sources of power consumption –Power dissipation in CMOS inverter –Basic principle of low power design.

UNIT II POWER EFFICIENT METHODS **9**

Logic level power optimization –Circuit level low power design –Gate level low power design – Architecture level low power design –VLSI subsystem design of adders, multipliers, and PLL

UNIT III LOW POWER CMOS CIRCUIT DESIGN **9**

Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories –low power clock –Advanced techniques –Lector Technique for leakage reduction, Adiabatic techniques –Physical design, Floor planning, placement and routing.

UNIT IV POWER COMPUTATION **9**

Power Estimation techniques, circuit level, gate level, architecture level, behavioral level, –logic power estimation –Simulation power analysis –Probabilistic power analysis

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER **9**

Synthesis for low power –Behavioral level transform –Algorithms for low power –software design for low power.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to find the power dissipation of MOS circuits
CO2: Ability to design and analyse various MOS logic circuits
CO3: Ability to apply power efficient techniques for low power dissipation
CO4: Ability to estimate the power dissipation of ICs
CO5: Ability to develop algorithms to reduce power dissipation by software

REFERENCES:

1. Kaushik Roy and S.C Prasad, " Low Power CMOS VLSI Circuit Design" Wiley, 2009
2. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
3. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer, October 2012.
4. Gary Yeap, "Practical low power digital VLSI design", Kluwer, October 2012.
5. Abdelatif Belaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, September 2012.

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6. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, JohnWiley and sons,inc. 2001.
7. J.Rabaey, “Low Power Design Essentials (Integrated Circuits and Systems)”, Springer, 2009.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	3	3	2	1	-
CO2	3	3	3	3	1	-
CO3	3	3	3	3	1	-
CO4	3	3	3	3	1	-
CO5	3	3	3	3	1	-
AVG	15/5=3	15/5=3	15/5=3	14/5=2.8	5/5=1	-

VE3016 SOLID STATE DEVICE MODELING L T P C
3 0 0 3

UNIT I MOSFET DEVICE PHYSICS 9

Introduction to solids, Bonding forces and energy bands in solid semiconductors, MOS capacitor - Interface Charge, threshold voltage, MOS Capacitance, MOS Charge control model, MOS Operation and characteristics. MOSFET fabrication process.

UNIT II MOSFET MODELING 9

Basic MOSFET Modeling-Meyer model, velocity saturation model, capacitance model, Basic small signal model. Advanced MOSFET Modeling-modeling approach, High field effects, short channel effects, Gate leakage and effective oxide thickness, Unified MOSFET C–V Model- Unified Meyer C–V model, Ward–Dutton model, Non-quasi-static modeling.

UNIT III RF AND NOISE MODELING 9

RF modeling of MOS transistors- Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling. Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, modeling for accurate distortion analysis-nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuit.

UNIT IV BSIM4 MOSFET MODELING 9

Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, Mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, Noise model, Junction diode models , Layout-dependent parasitics model.

UNIT V OTHER MOSFET MODELS 9

The EKV model- model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, temperature effects, MOS model 9, MOSAI model, Influence of process variation, Modeling of device mismatch for Analog/RF Applications.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the concepts and procedural flow that are used to construct the complicated device

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models

CO2: Design and analyze different MOSFET models

CO3: Analyze the noise models of MOSFET

CO4: Analyze the design challenges involved in device models

CO5: Analyze the EKV and BSIM4 MOSFET models

REFERENCES:

1. Rudan, Massimo, “Physics of Semiconductor Devices”, Springer International Publishing, 2017
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, 2nd Edition, Tata McGraw Hill, 2017
3. Yannis Tsividis and Colin McAndrew, “Operation and Modelling of the MOS transistor”, Cambridge University Press, 2011.
4. B. Bhattacharyya, “Compact MOSFET Models for VLSI Design”, John Wiley & Sons Inc., 2009.
5. Streetman and Banerjee, Semiconductor Physics and Devices, 6th Edition, Pearson Prentice Hall, 2006.
6. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd, 2003

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	3	3	2	1
CO2	3	1	3	3	2	1
CO3	3	1	3	3	2	1
CO4	3	1	3	3	2	1
CO5	3	1	3	3	2	1
AVG	15/5=3	5/5=1	15/5=3	15/5=3	10/5=2	5/5=1

VE3017 **NETWORK ON CHIP DESIGN** **L T P C**
3 0 0 3

UNIT I INTRODUCTION TO INTERCONNECTIONNETWORKS **9**

Uses of Interconnection Networks, Network Basics, A Simple Interconnection Network, Network Specifications and Constraints, Topology, Routing, Flow Control, Router Design, Performance Analysis. Case Study: The SGI Origin 2000

UNIT II TYPES OF NETWORKS **9**

Butterfly Networks, Torus Networks Mesh Networks, Non-blocking networks, Non-interfacing networks, Crossbar networks Clos Networks, Bene˘s Networks, Sorting Networks. Case Study: The BBN Butterfly

UNIT III ROUTING & FLOW CONTROL **9**

Routing Basics, Deterministic Routing, Dimension-Order Routing, Adaptive Routing, Adaptive Routing Basics, Minimal Adaptive Routing, Fully Adaptive Routing.Flow control basics, Butterflow control, Buffer Management and Back pressure, A flit reservation flow control, Deadlock and livelock avoidances, Deadlock and livelock avoidances in adaptive routing

UNIT IV QUALITY OF SERVICE & ROUTER **9**

Guranteed services, Best-Effort services, Router Datapath Components, Input Buffer organization, Switches, Output Organization, Arbitration, waveform allocator,Processor-Network Interface, SharedMemory Interface. Case Study: ATM Service Classes

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UNIT V PERFORMANCE ANALYSIS 9

Throughput, Latency, Fault Tolerance, Common Measurement Pitfalls Queuing Theory, Probabilistic Analysis, Application-Driven Workloads, Synthetic Workloads, Virtual Channels, Network Size, Injection Processes, Prioritization, Stability, Fault tolerance.Case Study: Efficiency and Loss in the BBN Monarch Network

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design various networks by considering design constrains
CO2: Design and Analyze the various types of networks
CO3: Design the routing and flow control in networks
CO4: Analyze the various performance metrics
CO5: Design the quality of service and routing mechanisms

REFERENCES:

1. Santanu Kundu Santanu Chattopadhyay, " Network-on-Chip - The Next Generation of System-on-Chip Integration", CRC Press, Taylor & Fracis Group, 2015.
2. Umit Y. Ogras and Radu Marculescu, " Modeling, Analysis and Optimization of Network-onChip Communication Architectures", Springer, 2013.
3. Stavroula N.Ventoura, "NOC Switch Design and Simulation using Matlab's Simulink", Master Thesis, National And Kapodistrian University of Athens, 2013.
4. Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures - System on Chip Interconnect", Elsevier, 2010.
5. Jih-Sheng Shen and Pao-Ann Hsiung, "Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication", IGI global, 2010.
6. William James Dally and Brian Patrick Towles, "Principles and Practices of Interconnection Networks",The Morgan Kaufmann Series in Computer Architecture and Design,2004

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	2	2	1	1
CO2	3	1	2	2	1	1
CO3	3	1	2	2	1	1
CO4	3	1	2	1	2	1
CO5	3	1	3	2	1	1
AVG	15/5=3	5/5=1	11/5=2.2	9/5=1.8	6/5=1.2	5/5=1

VE3018 DISTRIBUTED EMBEDDED COMPUTING L T P C
3 0 0 3

UNIT I THE HARDWARE INFRASTRUCTURE 9

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.

UNIT II INTERNET IN EMBEDDED COMPUTING 9

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

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UNIT III DISTRIBUTED COMPUTING USING JAVA 9

IO streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.

UNIT IV EMBEDDED AGENT 9

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent-Mobile robots.

UNIT V EMBEDDED COMPUTING ARCHITECTURE 9

Synthesis of the information technologies of distributed embedded systems – analog/digital co-design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the fundamentals of Network communication technologies
CO2: Analyze the internet and Java based networking
CO3: Design and analyze the network routing agents
CO4: Analyze the various network-on-chip technologies
CO5: Analyze the analog/digital co-design of distributed embedded computing architecture

REFERENCES:

1. Dietel & Dietel, “JAVA how to program”, Prentice Hall 2017.
2. Sape Mullender, “Distributed Systems”, Addison-Wesley,2nd edition,1993.
3. George Coulouris and Jean Dollimore, “Distributed Systems – concepts and design”,Addison Wesley 1988.
4. “Architecture and Design of Distributed Embedded Systems”, edited by Bernd Kleinjohann C-lab, Universitat Paderborn, Germany, Kluwer Academic Publishers, Boston, April 2001
5. M. Teresa Higuera-Toledano and Andy J. Wellings, " Distributed, Embedded and Real-time Java Systems", Springer, 2012.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	1	3	3	1	2
CO2	3	1	3	2	1	1
CO3	3	1	2	2	1	1
CO4	3	1	2	1	1	1
CO5	3	1	2	1	1	1
AVG	15/5=3	5/5=1	12/5=2.4	9/5=1.8	5/5=1	6/5=1.2

VE3019 EMBEDDED AUTOMOTIVE SYSTEMS L T P C
3 0 0 3

UNIT I SYSTEMS APPROACH TO CONTROL AND INSTRUMENTATION 9

System, Linear system theory, Steady-State sinusoidal frequency response of a system, State variable formulation of models, Control theory, Stability of Control System, Closed-Loop Limit-

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Cycle Control, Instrumentation, Basic Measurement System, Filtering, Digital Subsystem, Sinusoidal Frequency Response, Discrete Time Control System, Closed loop control, Example Discrete Time

UNIT II FUNDAMENTALS OF ELECTRONICS, MICROCOMPUTER INSTRUMENTATION AND CONTROL 9

Semiconductor Devices, Transistors, ICs, Operational Amplifiers, Use of Feedback in Op Amps, Phase-Locked Loop, Digital Circuits, Logic Circuits (Combination and Sequential Circuits), Timers and Counters, Microcomputer fundamentals, Tasks and Operations, CPU Registers, Reading Instructions, Programming Languages, Microcomputer Hardware, Microcomputer Applications in Automotive Systems, Instrumentation Applications of Mirocomputers, Microcomputers in Control Systems

UNIT III SENSORS, ACTUATORS AND ELECTRONIC ENGINE CONTROL 9

Motivation for Electronic Engine Control, Exhaust Emissions, Fuel Economy, Test Procedures, Concept of an Electronic Engine Control System, Engine Performance Terms, Exhaust Catalytic Convertors, Electronic Fuel-Control System, Analysis of Intake Manifold Pressure, Idle Speed Control, Electronic Ignition, Automotive Control System Applications of Sensors and Actuators, Throttle Angle Sensor, Temperature Sensor, Coolant Sensor, Sensors for Feedback control, Knock Sensors, Automotive Engine Control Actuators, Variable Valve Timing, Electric Motor Actuators, Ignition System.

UNIT IV MOTION AND DIGITAL POWERTRAIN CONTROL SYSTEM 9

Digital Engine Control, Features, Control Modes for Fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Electronic Ignition Control, Integrated Engine Control System, Summary of Control Modes, Cruise Control System, Cruise Control Electronics, Antilocking Braking System, Electronic Suspension System, Electronic Steering Control, Four-Wheel Steering

UNIT V AUTOMOTIVE INSTRUMENTATION, TELEMATICS AND ITS DIAGNOSTICS 9

Modern Automotive Instrumentation, Input and Output Signal Generation, Advantages of Computer Based Instrumentation, Display Devices, Flat Panel Display, Fuel Quantity Measurement, Coolant Temperature Measurement, Oil Pressure Measurement, Vehicle Speed Measurement, High-Speed Digital Communication (CAN BUS), Telematics, GPS Navigation, GPS System Structure, Automotive Diagnostics.

TOTAL: 45 PERIODS

PROGRESS THROUGH KNOWLEDGE

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze with the fundamentals of Electronic Components related to automotive applications
CO2: Design Automotive Sensors, Actuators and Instrumentations
CO3: Analyze the Control Mechanisms in an Automotive System
CO4: Analyze the operations of Telematics and Diagnostic methods
CO5: To be able to understand the complete automotive operation and control mechanisms

REFERENCES:

1. Al. Santini ,“Automotive Electricity and Electronics”,Second Edition, Delmar Cengage Learning, 2013.
2. William B. Ribbens, “Understanding Automotive Electronics- An Engineering Prespective”, 7th Edition, Butterworth-Heinemann Publications, 2012.
3. Robert Bosch,” Automotive Hand Book”, SAE, 5TH Edition,2000.

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4. Young A.P. & Griffiths, " Automotive Electrical Equipment" , ELBS & New Press,1999.
5. Bechhold, " Understanding Automotive Electronic", SAE,1998.
6. Tom Weather Jr. &Cland c. Ilunter, " Automotive computers and control system", Prentice Hall Inc., New Jersey,1984
7. Crouse W.H., " Automobile Electrical Equipment" , McGraw Hill Co. Inc., New York ,1995.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	2	1	2	1	1	3
CO2	3	1	3	3	3	1
CO3	2	1	3	3	3	1
CO4	2	1	3	3	3	1
CO5	3	1	3	3	1	1
AVG	12/5=2.4	5/5=1	14/5=2.8	13/5=2.6	11/5=2.2	7/5=1.4

NE3052 COMPUTATIONAL INTELLIGENCE L T P C
3 0 0 3

UNIT I NEURAL NETWORKS 9

Biological Neurons Networks - Artificial Neural Networks - Supervised - Unsupervised learning - Reinforcement Learning -Hebb learning- Perceptrons- Back Propagation networks -Radial Basis Function Networks-Adaptive Resonance architectures -Support Vector Machines

UNIT II FUZZY LOGIC 9

Fuzzy Sets - Operations on Fuzzy Sets - Fuzzy Relations - Membership Functions - Fuzzy RulesandFuzzyReasoning-FuzzyInferenceSystems-FuzzyExpertSystems-Fuzzy Decision Making

UNIT III NEURO-FUZZYMODELING 9

Adaptive Neuro-Fuzzy Inference Systems-Coactive Neuro –Fuzzy Modeling-Classification and Regression Trees-Data Clustering Algorithms-Hybrid learning algorithms-Applications of Neuro-fuzzy concepts

UNIT IV DEEP LEARNING NETWORKS 9

Introduction to Deep neural networks-Convolution neural networks-Deep Belief Networks-Recurrent neural networks – Case studies

UNIT V EVOLUTIONARY ALGORITHMS 9

Heuristic search and optimization techniques-Introduction to Genetic Algorithms-Social Algorithms – Ant colony Optimization- Particle swarm Optimization - Case studies

COURSE OUTCOMES:

On completion of the course the student should be able to

CO1: Design systems based on neural network architectures
CO2: Perform basic operations in fuzzy and design fuzzy systems
CO3: Implement neuro - fuzzy models for various applications
CO4: Design and implement deep learning architectures
CO5: Design optimization-based algorithm for various application

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REFERENCES:

1. Lan Good fellow, Yoshua Bengio and Aaron Courville, “DeepLearning” The MIT Press, Cambridge,2016.
2. Jyh-ShingRogerJang,Chuen-TsaiSun,EijiMizutani,“Neuro-uzzy and Soft Computing”, Pearson Edn., 2015.
3. George J.Klir and BoYuan, “FuzzySetsand Fuzzy Logic-Theory and Applications”, Prentice Hall, 2011.
4. David E. Goldberg, “Genetic Algorithms in Search, Optimization and Machine Learning”, Pearson Education, 2008.
5. James A. Freeman and David M. Skapura, “Neural Networks Algorithms, Applications, and Programming Techniques”, Pearson Edn., 2003.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	3	2	3	1	1	1
CO2	3	2	3	1	1	1
CO3	3	2	3	2	2	2
CO4	3	2	3	2	3	3
CO5	3	2	3	2	3	3
AVG	15/3=3	10/5=2	15/5=3	8/5=1.6	10/5=2	10/5=2

NE3054 ELECTROMAGNETIC INTERFERENCE AND ELECTROMAGNETIC COMPATIBILITY **L T P C**
3 0 0 3

UNIT I EMI/EMC CONCEPTS **9**

EMI/EMC Concepts - EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI,ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES **9**

EMI Coupling Principles-Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ;Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES **9**

EMI Control Techniques , Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transients suppressors,Cable routing,Signal control.

UNIT IV EMC DESIGN OF PCBs **9**

EMC Design Of PCBs -Component selection and mounting;PCB trace impedance; Routing;Crosstalk control;Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENT AND STANDARDS **9**

EMI Measurements And Standards- Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined an echoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards -CISPR, FCC, IEC, EN; Military standardsMIL461E/462.

TOTAL:45 PERIODS

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COURSE OUTCOMES:

On completion of the course the student should be able to

CO1: Understand EMI and susceptibility

CO2:Identify EMI coupling mechanisms

CO3: Use appropriate EMI control schemes in electronic systems

CO4:Design PCBs with EMC

CO5: Conduct EMI measurements according to standards.

REFERENCES:

1. C.R.Paul,"Introduction to Electromagnetic Compatibility",John Wiley and Sons,Inc,3rd Edition,2022
2. David A Weston,"Electromagnetic Compatibility—Methods,Analysis,circuits and measurements" CRC press, Bocaraton2017
3. Tim Williams,"EMC for product designers",Newness,5thEdition,2017.
4. PatrickG.Andre and Kenneth Wyatt," EMI Trouble shooting Cook book for Product Designers ,Sci Tech publishing,2014
5. Henry W.Ott.,"Electromagnetic Compatibility Engineering, Revised edition, Wiley Black well Newyork,2009.

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO1	2	1	2	2	2	2
CO2	3	1	3	3	3	3
CO3	3	1	3	3	3	3
CO4	3	1	3	3	3	3
CO5	3	1	3	3	3	3
AVG	14/5=2.8	5/5=1	14/5=2.8	14/5=2.8	14/5=2.8	14/5=2.8

WT3058 SIGNAL INTEGRITY FOR HIGH-SPEED ELECTRONIC SYSTEMS L T P C

3 0 0 3

UNIT I FUNDAMENTALS OF ELECTROMAGNETICS 9

The Basics - Maxwell's Equations, Common Vector Operators - Wave Propagations Electrostatics - Magneto statics - Power flow and the Poynting Vector - Reflections of Electromagnetic Waves.

UNIT II CROSS TALK AND NON IDEAL CONDUCTOR MODELS 9

Mutual Inductance and Capacitance - Coupled Wave Equations - Coupled Line Analysis - Modal Analysis - Crosstalk Minimization - Signals Propagation in Unbounded Conductive Media - Classic Conductor Model for Transmission models

UNIT III DIELECTRIC MATERIALS 9

Polarization of Dielectrics - Classification of Dielectric Materials - Frequency Dependent Dielectric Behavior - Fiber Weave Effect - Environmental Variation in Dielectric Behavior Transmission Line Parameters for Lossy Dielectrics and Realistic Conductors.

UNIT IV DIFFERENTIAL SIGNALING 9

Removal of Common Mode Noise - Differential Crosstalk - Virtual Reference Plane - Propagation of Modal Voltages - Common Terminology - Drawbacks of Differential Signaling.

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UNIT V CHANNEL AND I/O CIRCUITS MODELLING 9

Creating a Physical Transmission Line Model - Non idea Return Paths - I/O Design Considerations - Push-Pull Transmitters - CMOS Receivers - ESD Protection Circuits - On Chip Termination - Bergeron Diagrams.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students should be able to

CO1: Understand the fundamental concepts of signal integrity in high speed PCBs.
CO2: Identify and resolve crosstalk.
CO3: Interpret the frequency dependence of dielectrics.
CO4: Analyze the design considerations in I/O circuits.
CO5: Comprehend transmission line model.

REFERENCES:

1. Stephen H. Hall, Howard L. Heck, “Advanced Signal Integrity for High-Speed Digital Designs”, Second Edition, John Wiley and Sons, 2009.
2. Mike Peng Li, “Jitter, Noise, and Signal Integrity at High-Speed”, First Edition, Prentice Hall, 2007.
3. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, First Edition, Prentice Hall PTR, 2003.
4. James Edgar Buchanan, “Signal and power integrity in digital systems: TTL, CMOS, and BiCMOS”, Second Edition, McGraw-Hill, 1996.
5. H. W. Johnson and M. Graham, “High-Speed Digital Design: A Handbook of Black Magic”, Second Edition, Prentice Hall, 1993.

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CO5	3	1	1	3	1	1
AVG	15/5=3	5/5=1	8/5=1.6	9/5=1.8	5/5=1	5/5=1

PROGRESS THROUGH KNOWLEDGE

Attested

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